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ELECTRONIC DESIGN

JUNE 27, 1994

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FOR ENGINEERS AND ENGINEERING MANAGERS—WORLDWIDE

CHIPS RESCUE BATTERY-POWERED SYSTEMS

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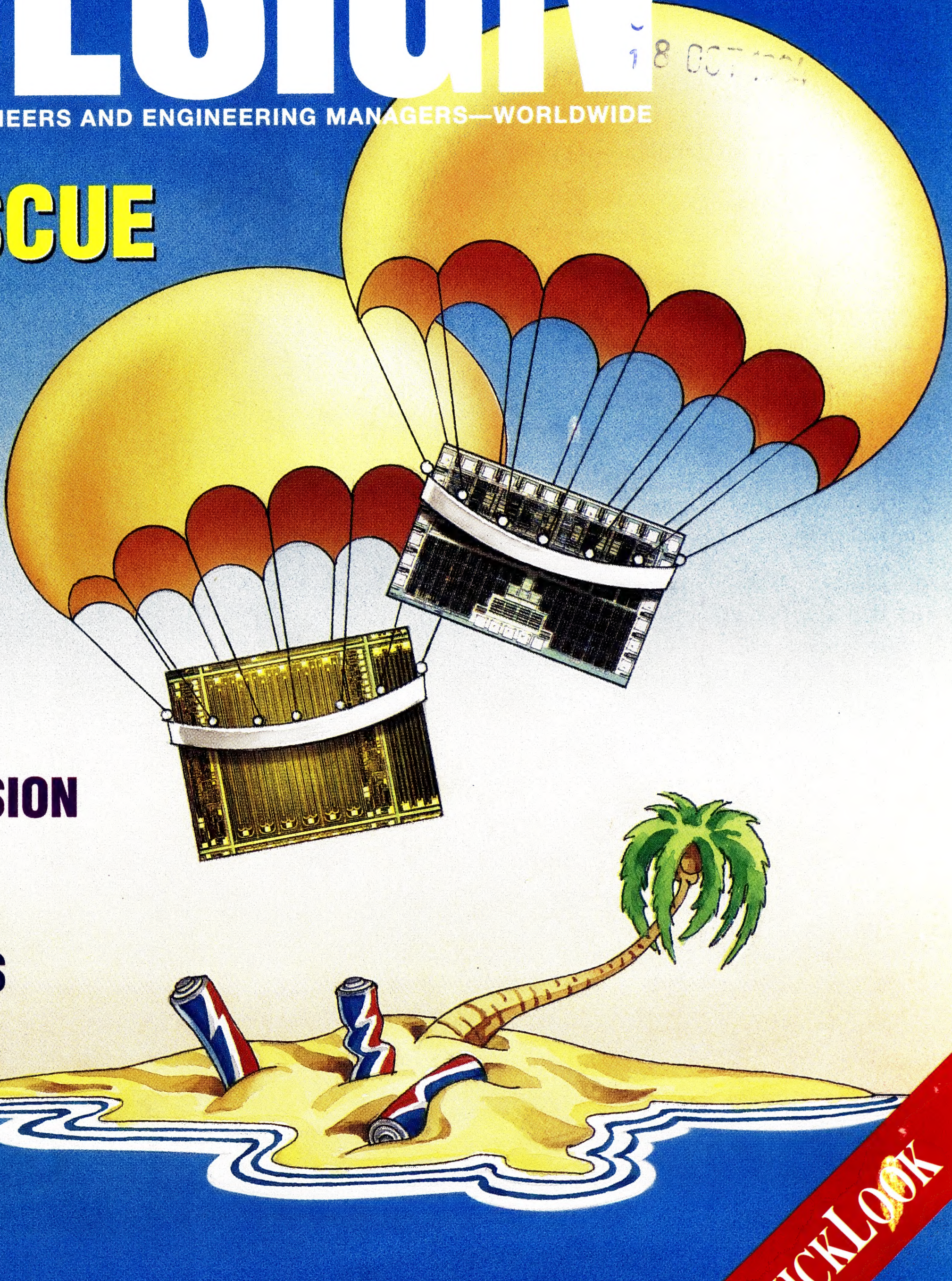
- KEEP QUALITY DESPITE FAST PRODUCT CYCLES
- PEASE PORRIDGE



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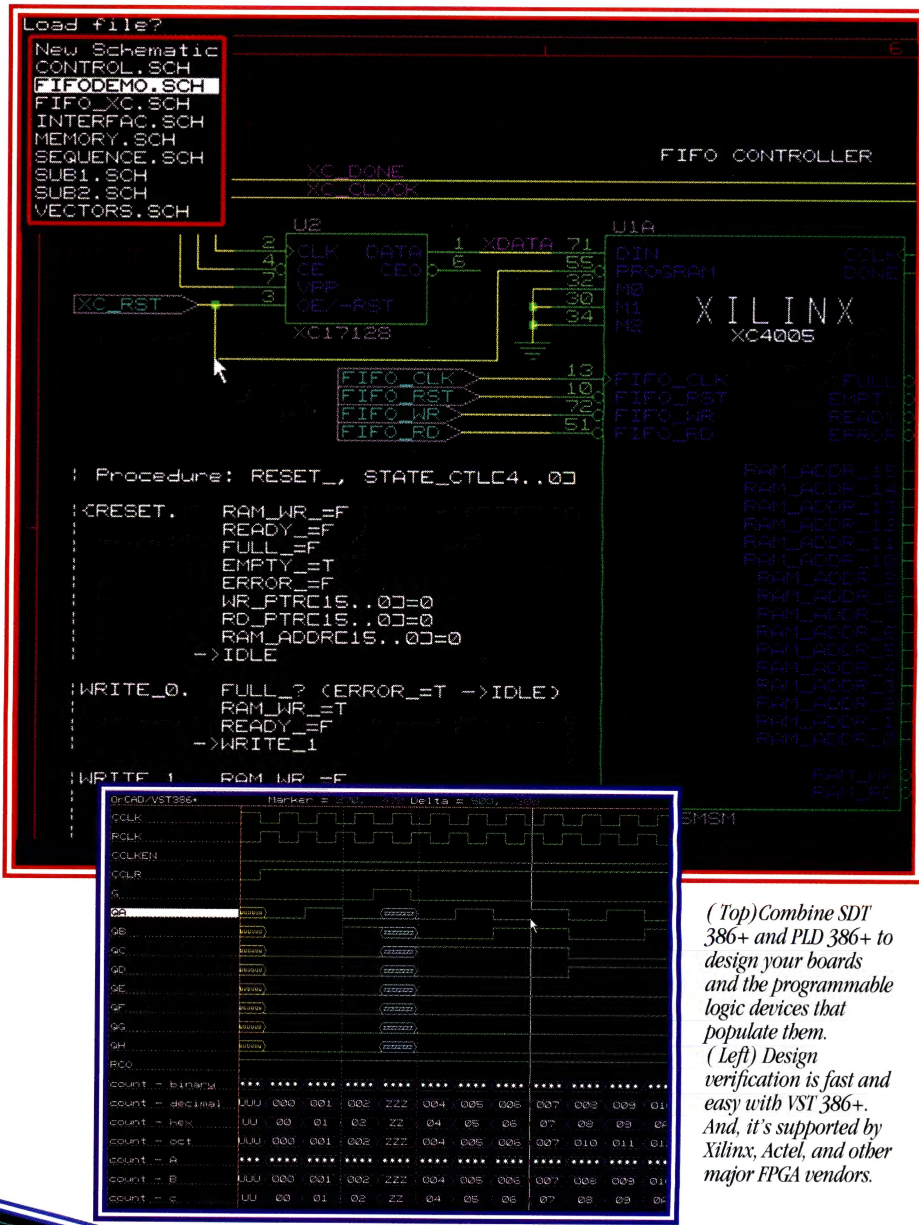


```
Load file?
New Schematic
CONTROL.SCH
FIFODEMO.SCH
FIFO_XC.SCH
INTERFAC.SCH
MEMORY.SCH
SEQUENCE.SCH
SUB1.SCH
SUB2.SCH
VECTORS.SCH
```

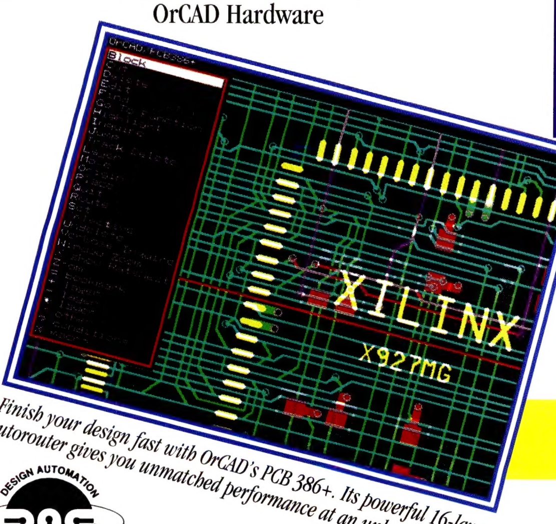
```
| Procedure: RESET_, STATE_CTL[4..0]

|<RESET.    RAM_WR_=F
|           READY_=F
|           FULL_=F
|           EMPTY_=T
|           ERROR_=F
|           WR_PTR[15..0]=0
|           RD_PTR[15..0]=0
|           RAM_ADDR[15..0]=0
|        ->IDLE

|WRITE_0.   FULL_? (ERROR_=T ->IDLE)
|           RAM_WR_=T
|           READY_=F
|        ->WRITE_1

|WRITE_1    RAM_WR_=F
```

(Top) Combine SDT 386+ and PLD 386+ to design your boards and the programmable logic devices that populate them.
(Left) Design verification is fast and easy with VST 386+. And, it's supported by Xilinx, Actel, and other major FPGA vendors.



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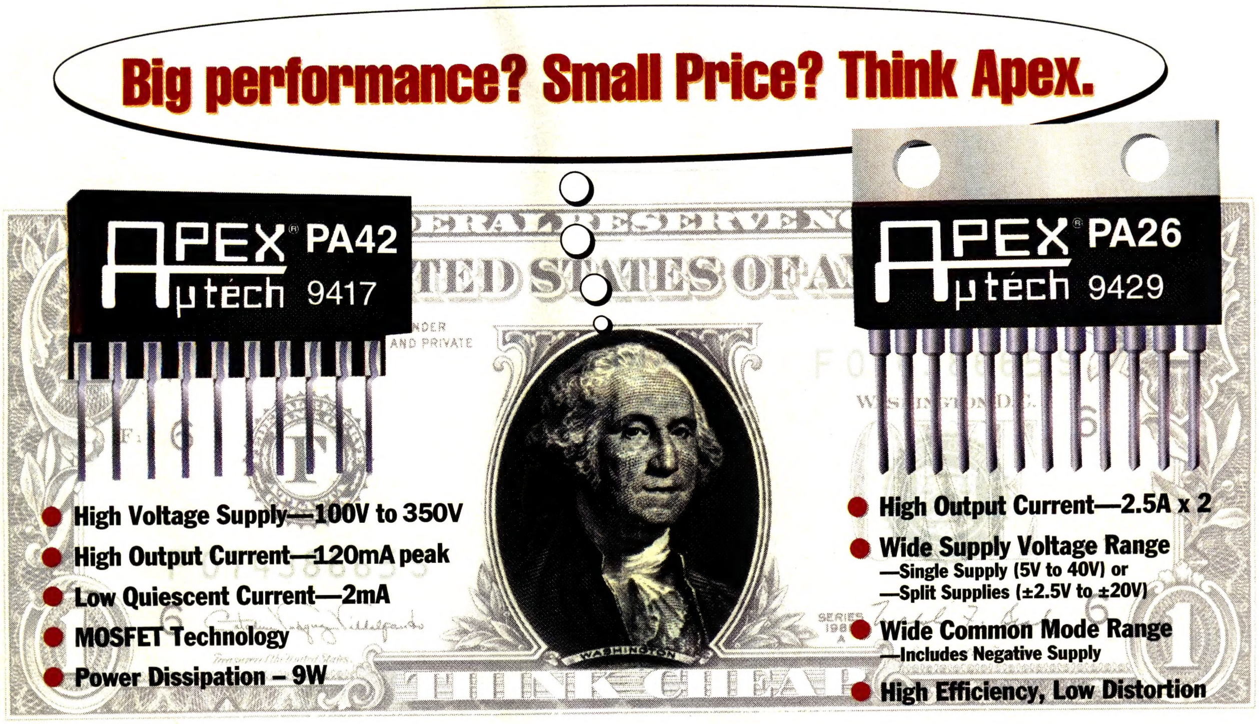

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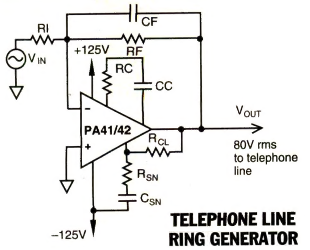

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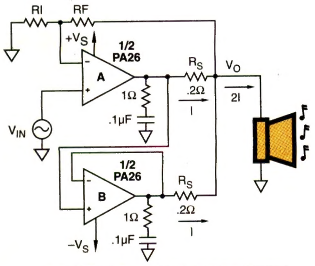
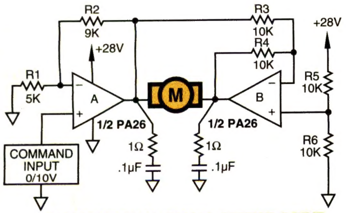


5A AUDIO PARALLEL CONNECTION



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KEY FEATURES/KEY SPECIFICATIONS

Part #	V_{SS}	I_O	V_{CM}	V_{SAT}	PKG	$/10K
PA26	5V-40V	2.5A x 2	$-V_S-.3V$	1.8V @ 1.0A	SIP[1]	$3.45
PA21M[2]	5V-40V	2.5A x 2	$-V_S-.3V$	3.5V @ 2.A	TO-3[1]	$39.54
PA42	100V-350V	120mA	$\pm V_S-12V$	10V @ 40mA	SIP[1]	$13.60
PA41M[2]	100V-350V	120mA	$\pm V_S-12V$	10V @ 40mA	TO-3[1]	$46.62

[1] The TO-3 is a hermetic package; the SIP is a non-hermetic package
[2] "M" designates hi-rel military grade

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For more demanding applications, Apex offers the **PA21M (PA26)** and the **PA41M (PA42)**. Both are housed in hermetically sealed TO-3 packages and tested over the full military case temp range of –55°C to +125°C.

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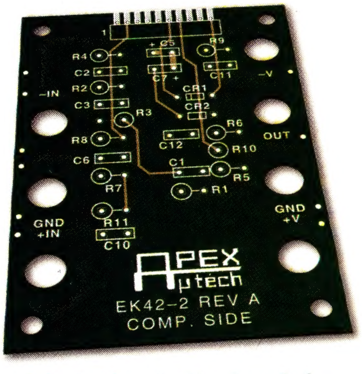

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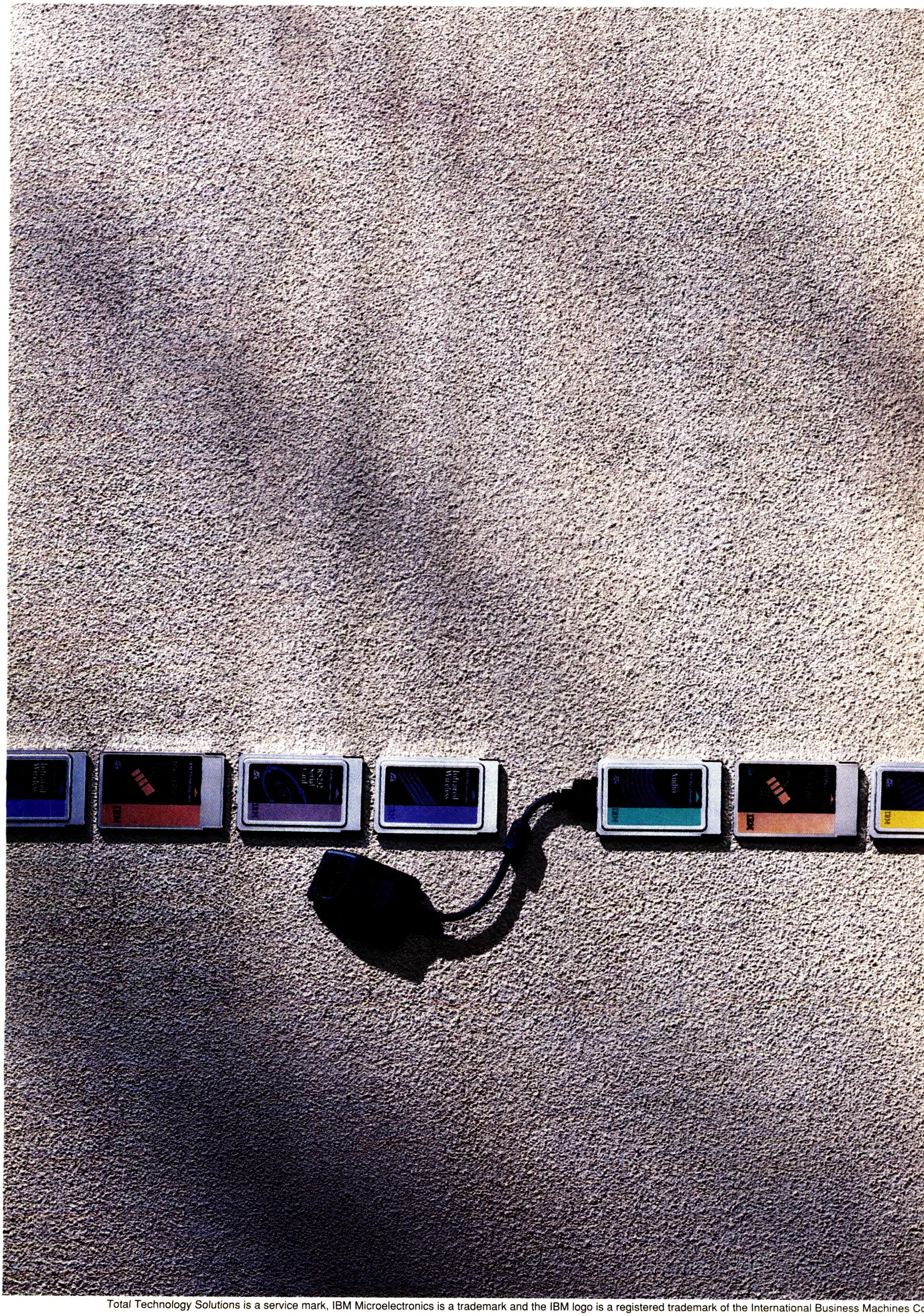

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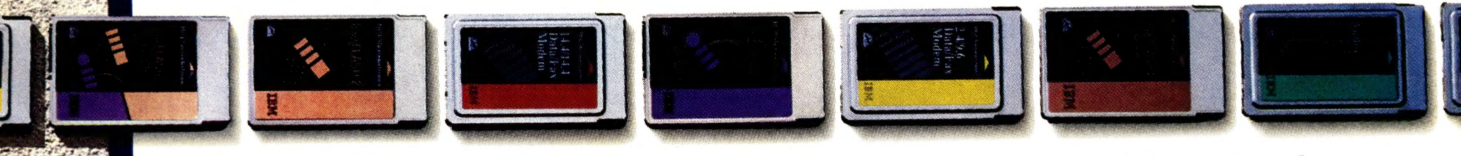
Everything we know about PCMCIA can be summed up in a single line.



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If you're looking for an OEM supplier who really understands the ins and outs of PCMCIA, the name to know is IBM Microelectronics™ Division.

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What's more, the performance of our PCMCIA products is just as impressive as their breadth. One example is our complete line of memory products, which features 1, 2 and 4MB Flash cards, 1 and 2MB SRAM cards with battery backup, combination Flash/SRAM cards, plus a full range of innovative Flash 2 cards offering non-volatile storage and low power consumption.

Another example of our PCMCIA know-how can be found in IBM Microelectronics' family of I/O, communications and networking products. Chief among them is a series of advanced data/fax modems, and RS232 serial cards that offer complete connectivity in a rugged, compact package. For users who want LAN connectivity, there's also a family of infrared wireless adapters that are simple to install and use.

Multimedia is yet another area where we put our PCMCIA experience on the line. A case in point is our 16-bit audio adapter, an IBM "first" that places high-definition stereo sound in the hands of notebook and laptop users.

Mobile users will also appreciate our line of solid state file cards, a mass storage solution that emulates hard disk drives in Type I and II form factors. And users who want to bridge mobile and desktop applications will no doubt approve of our versatile PCMCIA desktop adapter, a four slot device that accepts Type I, II and III PCMCIA cards.

Of course, leading the way in PCMCIA is nothing new to us. As a founding member of PCMCIA (the industry group responsible for setting future standards), we've demonstrated a strong commitment to innovation and quality since day one.

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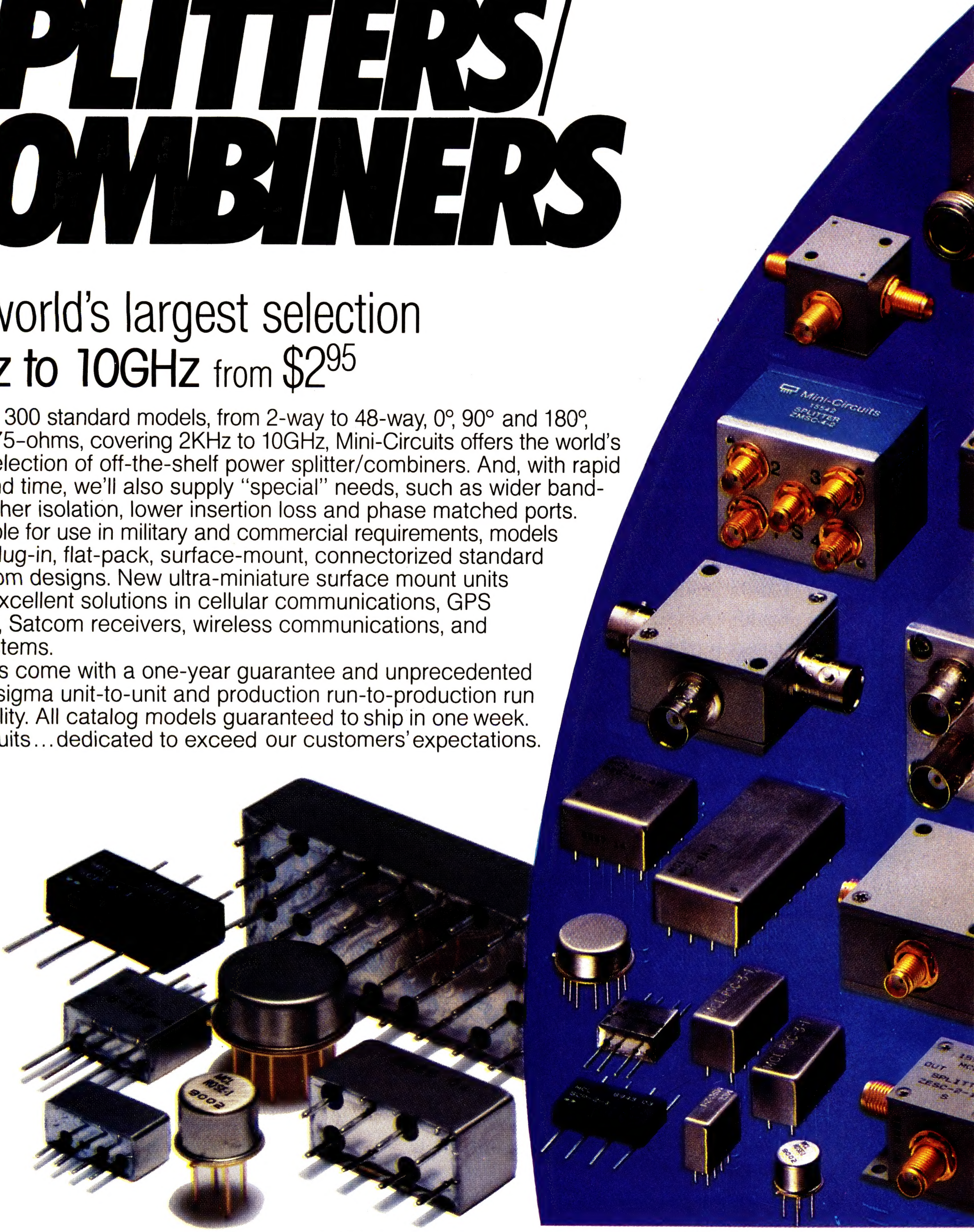

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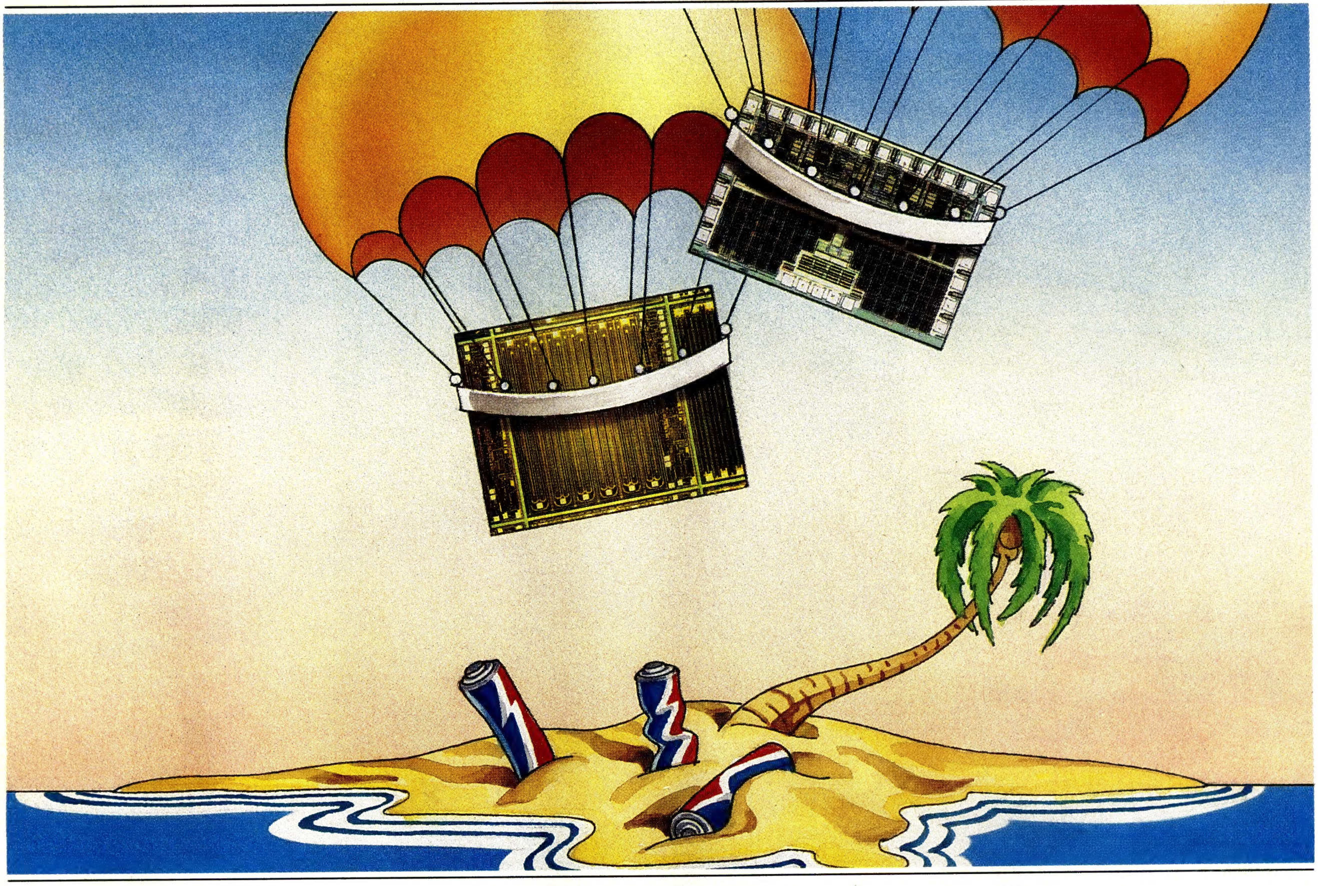

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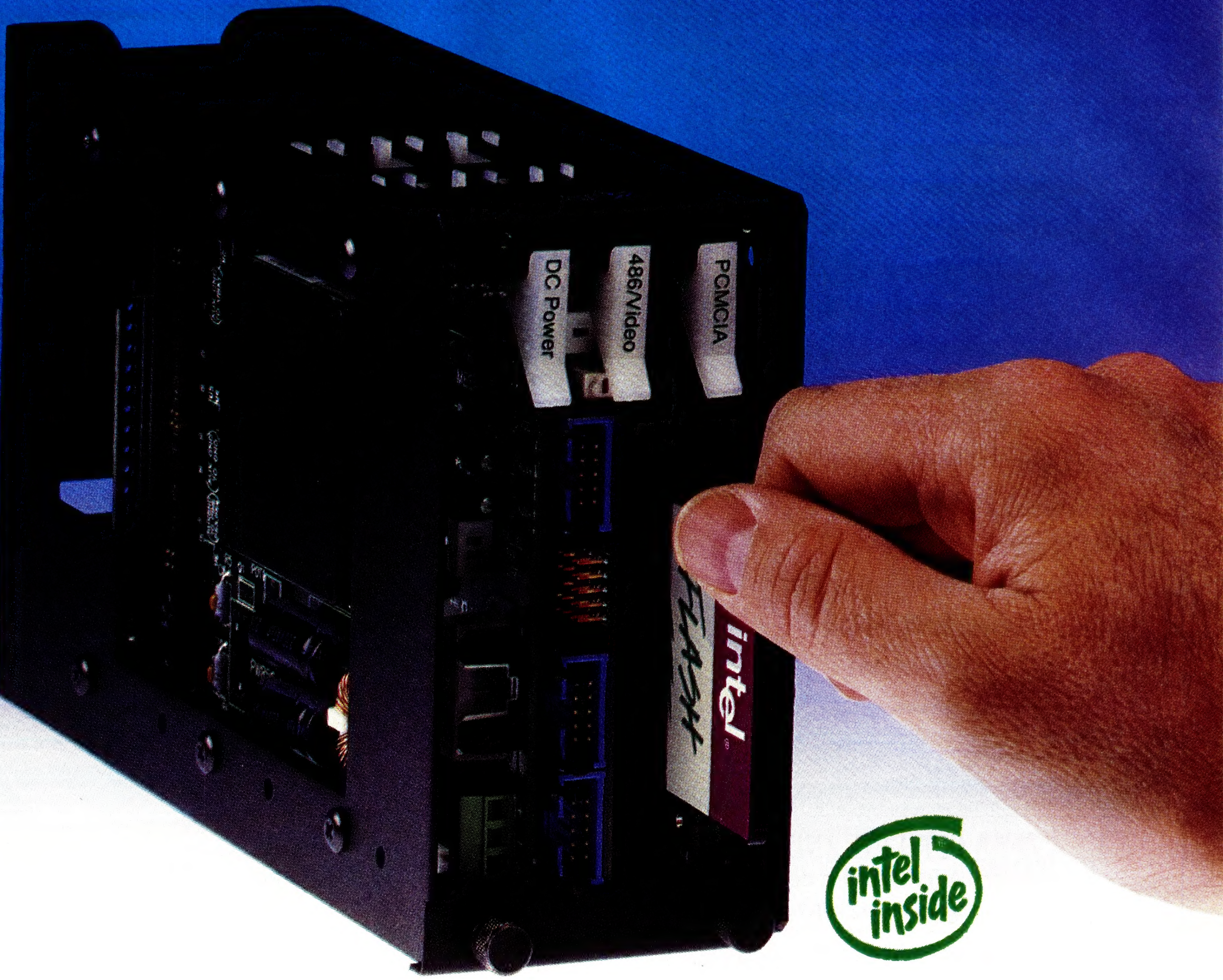

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ELECTRONIC DESIGN

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1975 Two Certificates of Merit
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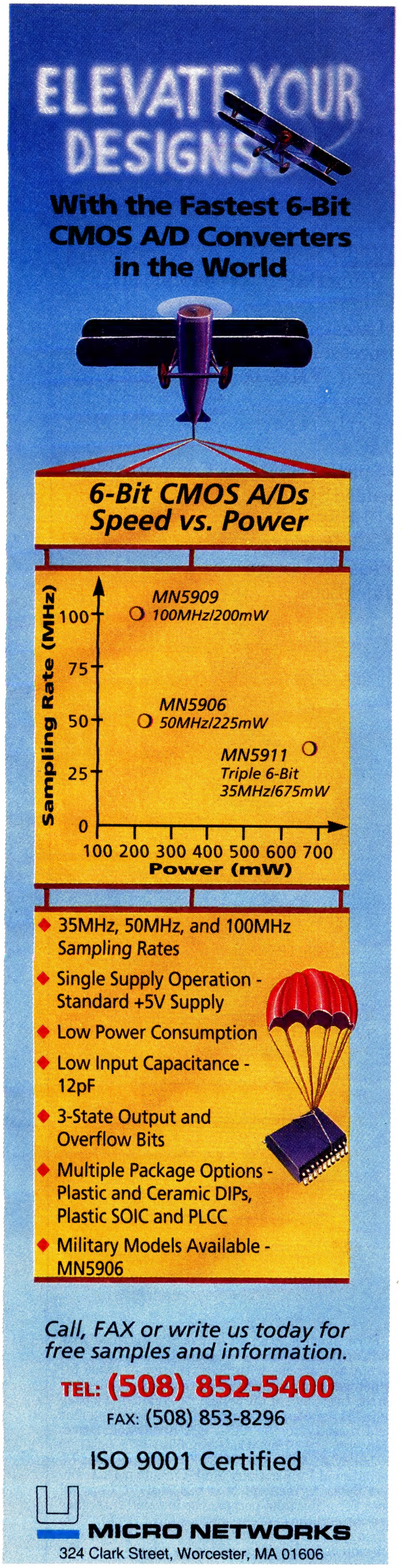

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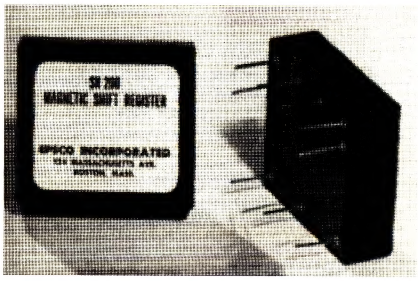
ELECTRONIC DESIGN 40 YEARS AGO

Magnetic Storage Elements Can Operate At Rates To 500kc

This line of encapsulated magnetic storage elements includes types which can be operated at rates up to 500kc. They are very reliable units designed to serve as storage elements, shift registers, and control elements. The typical unit illustrated at the right, Model SR-200, is a high speed unit using but one core per stored digit, and capable of working at rates up to 350kc. Designed for dip-solder assembly, its overall size is 9/16" x 1-5/8" x 1-7/8".



Some characteristics of this specific model include: 300 ma nominal shift current; 0.5-1.5μsec shift pulse width; 15v output signal amplitude; recommended diode (external): Transitron T6 or Raytheon CK742; recommended driving tube: RCA 6146 (as many as 50 magnetic storage elements may be driven by a single tube).

The Model SR-200 is also useful for circuit applications where it is desirable to replace vacuum tube circuitry with more reliable, less expensive magnetic elements; for example, by merely directly connecting the unit's input connections to the output, the unit will function as a continuous-readout flip-flop. Epsco Inc., Dept. ED, 126 Massachusetts Ave., Boston 15, Mass.*(Electronic Design, June 1954, p. 35.)*

Last month, we published an item on magnetic amplifiers. This device from Epsco is another example from the 1950s of efforts to exploit magnetic effects to perform circuit functions. Eventually, such devices were superseded by integrated circuits, but in their heyday of the 50s and 60s, they were solid-state alternatives to vacuum-tube circuitry. It was at Epsco, by the way, that the company's founder, Bernie Gordon, patented the successive-approximation analog-to-digital converter. Gordon later founded Analogic, where he is still active in analog technology. —SS

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The Types 600 and 601 Silicon Junction Diodes are characterized by high temperature stability and definite Zener voltage values. Constructed of single crystal silicon, the units have extremely low back currents ranging from 0.001 to 0.01μa at rated voltages. They have glass-to-metal hermetic seals. The minimum Zener voltage for the Type 601 is 50V. The minimum forward currents at 1V for the type 601 are 3ma and 2ma for ambient temperatures of 25°C and 150°C, respectively.

For the Type 601, the maximum inverse currents at –1v are 0.01μa and 20μa at 25°C and 150°C, respectively. At –10v, these currents are 0.04μa and 40 μa, respectively.

For the Type 600, the maximum inverse currents at 25°C for –1v and –10v are 1μa and 8μa, respectively. The maximum peak inverse operating voltage of the Type 600 is –30V. The minimum forward current for the Type 600 at 25°C and 1v is 3 ma.

These diodes are recommended for applications demanding either sharp Zener voltage characteristics or high-temperature stability. The cylindrically shaped units are about 1/2" long. Texas Instruments Inc., Dept. ED, 6000 Lemmon Ave., Dallas 6, Texas.*(Electronic Design, June 1954, p. 34.)*

With all due respect to California's Silicon Valley, we shouldn't forget that silicon got its start in commercial semiconductor devices about 1500 miles to the southeast, in Dallas. TI had procured its transistor manufacturing license from Western Electric in 1952 and soon after hired Bell Labs' Gordon Teal, who developed a process for growing single-crystal silicon. In late 1954, TI introduced the first commercial silicon transistors. Four years later, TI's Jack Kilby developed the first integrated circuit. At just about the same time, Fairchild Semiconductor's Bob Noyce (who co-founded Intel) developed the planar process for integrated circuits.—SS

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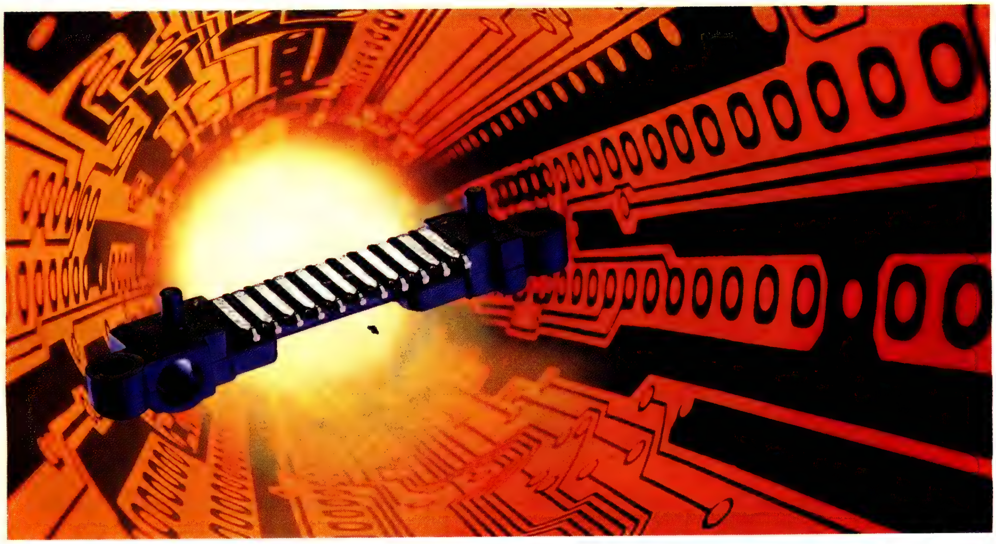

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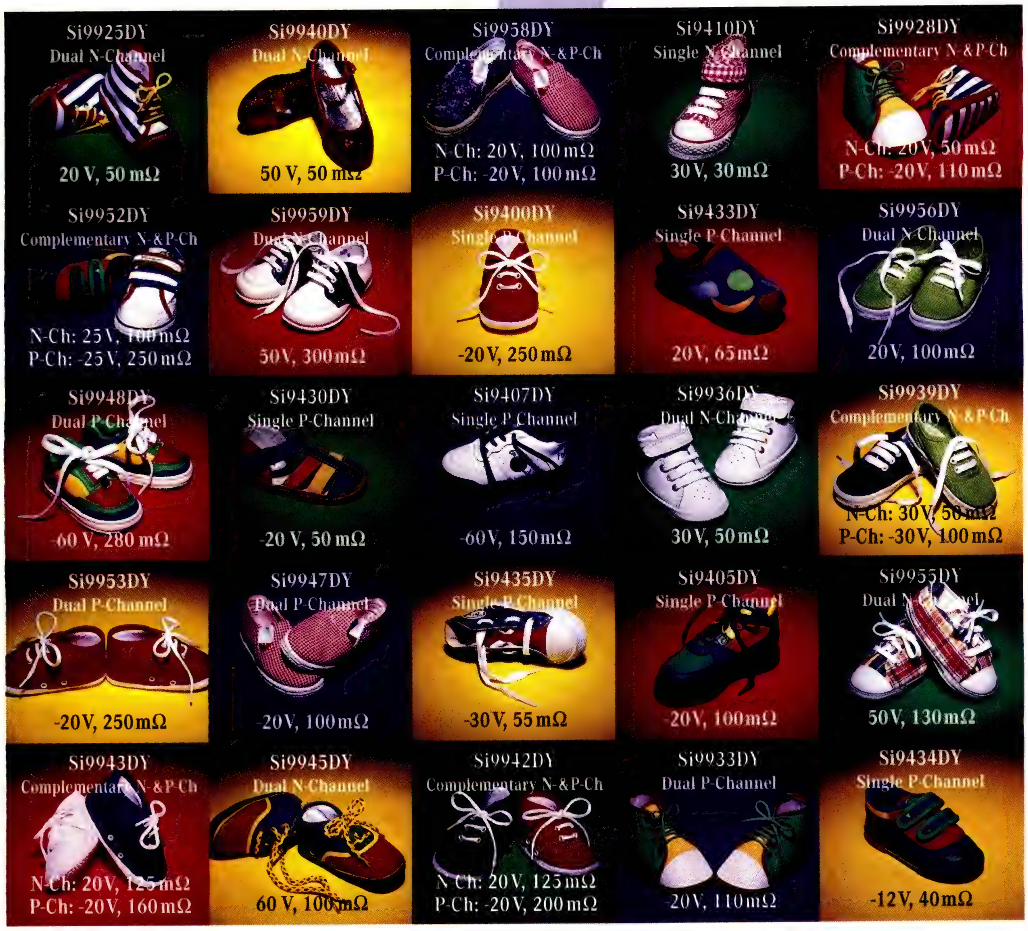

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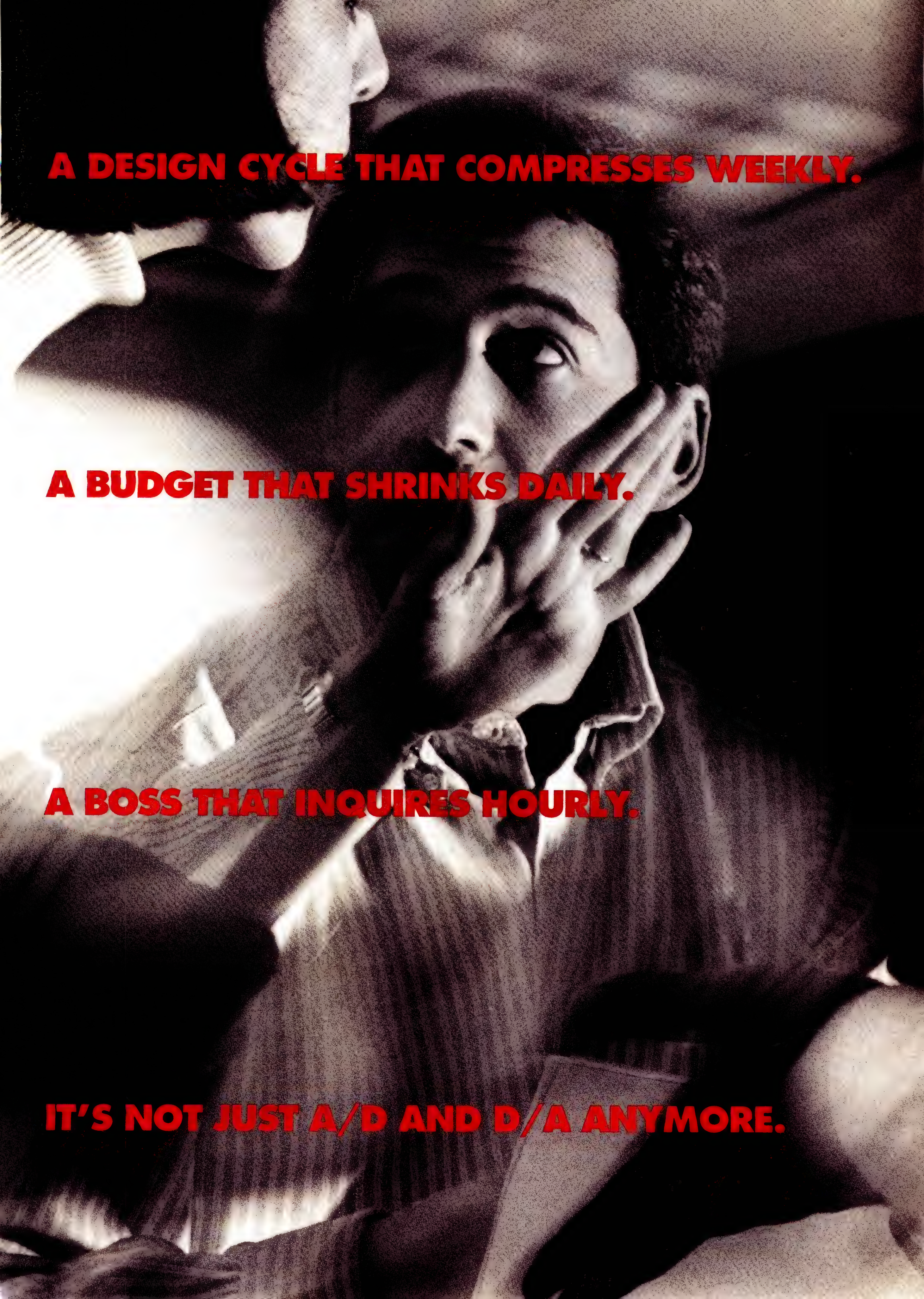
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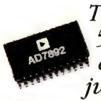

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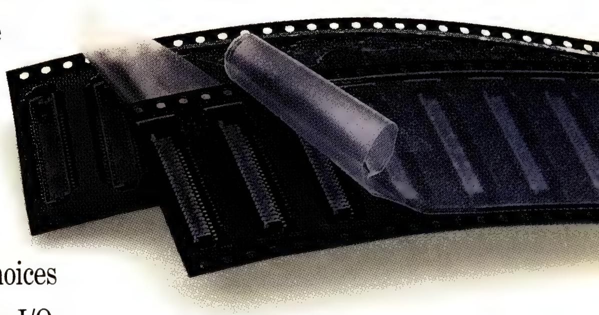

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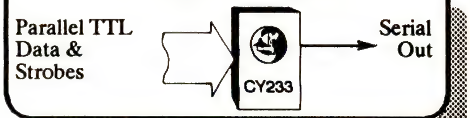

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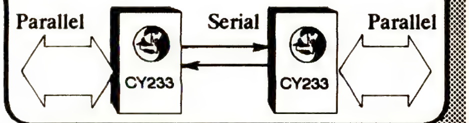

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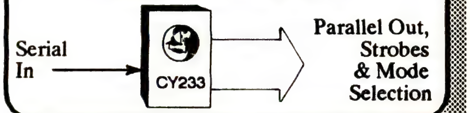

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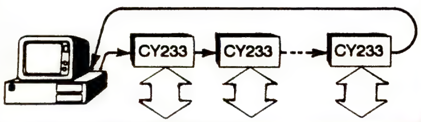

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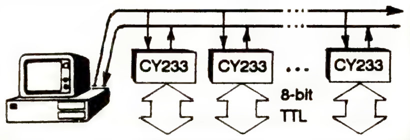

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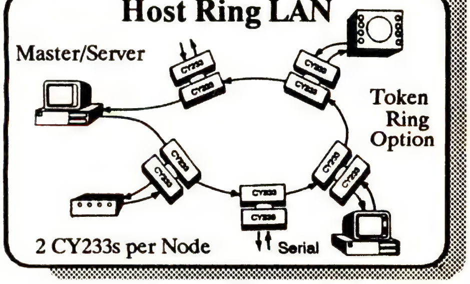

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READER SERVICE 184

THE FUTURE

Being an editor on a magazine that covers the electronics industry is, to say the least, an interesting job. I can't think of another industry that practically reinvents itself every few years. This is particularly good for software and computer companies, who find wonderful uses for new chips. Before multimedia came along, for example, I never would have considered buying a 1-Gbyte hard drive.

Hardly a month goes by without our hearing of at least one new revolutionary technology. Not all of these technologies actually start revolutions, of course. Some spawn a long line of product generations, such as Intel's 80x86 or Motorola's 680x0 microprocessors. That's not bad for the bottom line. It's also about as much as a company could hope for.

Other "revolutionary" technologies die of neglect. For example, I can think of at least three wireless local-area-network technologies that seem to have gone the way of the dinosaur.

Part of the job of our magazine is to help engineers figure out which technologies are going to be useful and which are going to end up in the trash heap. This is easier said than done, though. *Electronic Design* is primarily a technology-oriented magazine, and good technology can be pulled into the abyss by bad marketing, corporate politics, industry standards, competition, and even government intervention.

Our view is that the engineers and engineering managers who read this magazine are just as interested in their next design as they are in the current design. Design cycles are so short that this focus on the future is becoming a requirement for a successful company. That's why *Electronic Design* tries to help by taking a longer view that scans the technology horizon and isn't limited by the products in the market today.

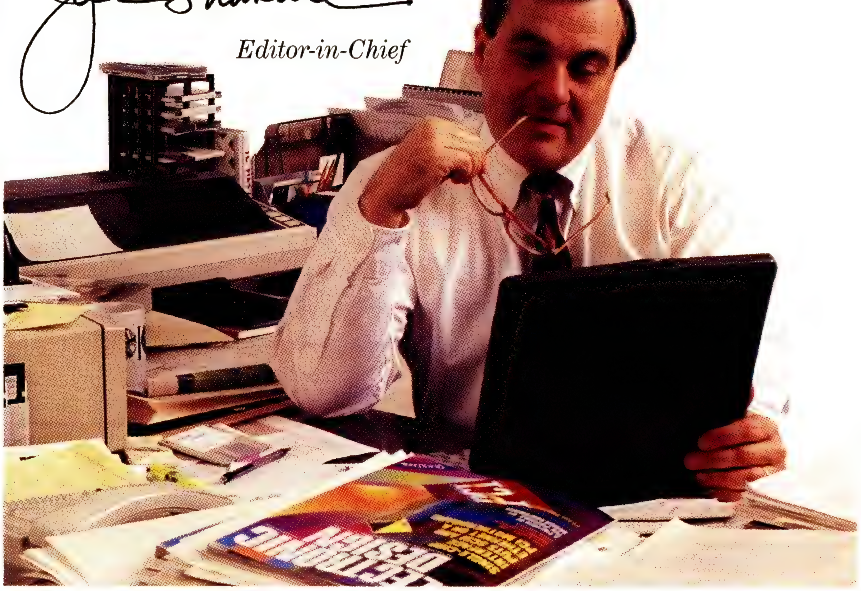
An important corollary to this theory is that we have confidence in our readers. If we're going to provide information that might help make their next design better, we can't be risk-adverse. No one can foresee the future.

Some of the new things we write about may not make the grade. In this regard, our reader is something like a baseball manager and *Electronic Design* is a dossier on minor-league prospects.

Not every player the minor-league scouts tout turns out to be a star. But it's better to have a scouting corps than to think you can play with the same team forever.

Josh Shandle

Editor-in-Chief



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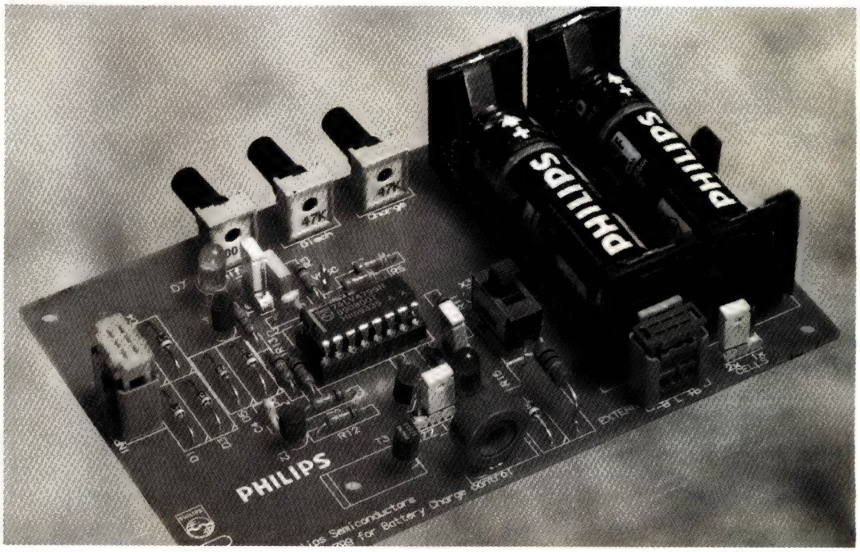
First low-voltage IC for economic NiCd and NiMH battery management

A new low-cost LV-HCMOS battery management IC, the 74LV4799, is the first of its kind to be designed for operation from supply voltages between 0.9 and 6 V so that it can be used with one to four rechargeable NiCd or NiMH cells. Intended for 'intelligent' batteries and applications with integrated batteries, the low-power device is ideal for use in domestic appliances, personal care products, cordless tools, personal communications, data handling and many other consumer applications.

An on-chip oscillator, divider and up/down counter maintain a highly accurate log of the battery status and the charge, self-discharge and discharge times. The IC features automatic switchover to trickle charge at the end of the charge time, and can be adjusted to support virtually all types of rechargeable batteries. Typical charging time is between four and 16 hours.



A demonstration board is available for evaluating the 74LV4799's performance in various battery charging applications and with different battery types.

Battery status indication includes an LED output for charge/battery full indication and a 'nearly empty' output for driving an LED or buzzer. The energy remaining can be detected by using the serial scan output, which represents the status of the internal counter. Built-in power-on reset initiates the IC when the battery is used for the first time or if it is disconnected. For maximum flexibility, the power-on sense input accepts input frequencies from DC to 100 kHz and voltages up to 10 V. The 74LV4799 is supplied in a 16-pin DIL package or in an SO minipack for surface mounting.

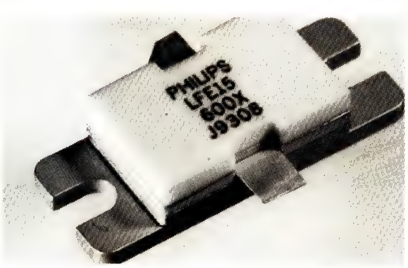
Reader Service 178

Single-ended silicon microwave transistor delivers 60 W

The LFE15600X silicon npn microwave power transistor is the first single-ended 60 W device suitable for use in the class AB output stages of transmitters operating in the 1.5 to 1.7 GHz frequency band. A similar transistor optimized for use in the 1.7 to 2.0 GHz band is under development and is scheduled for introduction during this year.

The LFE15600X's single-ended base input, plus its high power handling and diffused emitter resistors, allow transmitter powers of several hundred watts to be achieved by connecting a number of the devices in parallel, without the need for complex input-matching circuitry. The device's very low level of third-order intermodulation distortion, typically better than –30 dBc at 60 W PEP, suits it for use in multi-carrier transmitters such as those found in PCS base stations, as well as in transmitters for mobile satellite communications and digital audio broadcast systems.

The transistor achieves a typical full-power collector efficiency of 50% at a junction temperature of 100°C which results in lower operating temperatures and excellent long-term reliability. Typical power gain is 8.5 dB at 1.5 GHz, permitting simpler driver stage design.



The LFE15600X microwave power transistor is housed in an FO-231 metal/ceramic flanged package.

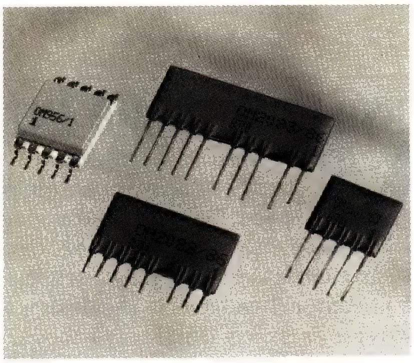
Reader Service 179

Philips
Semiconductors

High-gain wide-band amplifier modules for TV

High gain and excellent second order distortion figures are key features of Philips' new family of wide-band amplifier modules. All amplifiers are based on thin film hybrid technology giving excellent performance and stability, while laser trimming guarantees narrow tolerances on parameters. The OM208X family is intended for use in cable TV, main antenna TV and as general-purpose amplifiers for VHF and UHF applications, while the OM956/1 is designed for satellite TV amplifiers. This extension of the range of wide-band amplifiers gives OEMs the opportunity to choose an amplifier that exactly meets their requirements in terms of bandwidth, gain and output level.

The OM208X family comprises three basic modules, OM2081, OM2082 and OM2083, with one, two and three amplifier stages and typical gain figures of 10 to 12 dB, 19 dB and 29 to 30 dB respectively. Each type is available in two versions: one for the frequency range 40 to 600 MHz (OM208X/60) and the other for the range 40 to 860 MHz (OM208X/86). All modules are designed for a supply voltage of 12 V, have an output level of 105 dBμV for the second order and 115 dBμV for the third order at –60 dB intermodulation distortion, and a noise figure of 7.5 dB. Characteristic impedance of both input and output is 75 Ω. The modules are encapsulated in in-line, resin-coated packages, with five, nine and twelve pins respectively.


New high-gain wide-band hybrid amplifier modules are intended for TV and general purpose VHF and UHF applications.

The OM956/1, for satellite TV applications, has a frequency range of 860 to 2050 MHz. It has an output level of 112 dBμV for the third order at –35 dB intermodulation distortion and a gain of 18.5 to 21 dB, and is encapsulated in an SMD package.

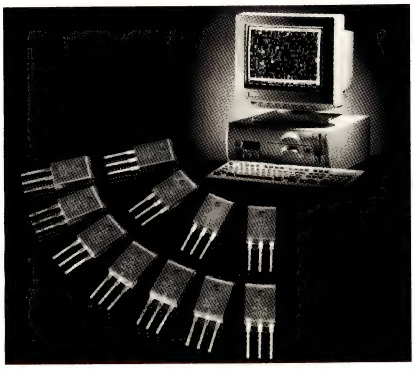
Reader Service 180

Horizontal deflection transistors enhance CRT monitor reliability

The short switching times and low power losses achieved by Philips Semiconductors' two new high-speed high-voltage npn power transistors significantly reduce power dissipation in the horizontal deflection circuits of CRT monitors. A narrow gain spread between transistors, resulting from carefully controlled diffusion processes, together with 100% testing of their RBSOA (reverse bias safe operating area) simplify the analysis of worst-case operating and fault conditions, allowing maximum circuit reliability to be designed-in. The BU2522AF and BU2527AF are targeted for use in 14- to 17-inch high-resolution monitors operating at horizontal scan rates up to 64 kHz.

The transistors are 1500 V devices designed to operate at mean collector currents between 5 and 7 A. Their DC maximum and peak collector current ratings are 10 A and 25 A respectively for the BU2522AF and 12 A and 30 A for the BU2527AF. When switching a mean current of 6 A in a 64 kHz horizontal deflection circuit, both transistors show a maximum charge storage time of only 2.0 μs, and maximum collector turn-off fall times are 0.25 μs for the BU2522AF and 0.20 μs for the BU2527AF. These very short switching times are major contributors to the low power dissipation and high reliability achievable.

The transistors are housed in SOT199 plastic power packages with electrically-isolated seating planes which eliminate the need for thermally-conductive washers between transistor and heat sink.

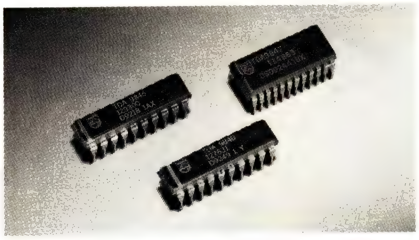

The BU2522AF and BU2527AF horizontal deflection transistors are easy to design-in for maximum reliability.

Reader Service 181

Stereo/dual sound processors for TVs and VCRs feature very reliable pilot identification

Three new stereo/dual sound processor ICs for TVs and VCRs all feature on-chip digital phase-locked loops, synchronous detectors and digital integrators to achieve extremely reliable identification of the stereo/dual sound pilot modulations. As a result, the use of these ICs eliminates any tendency for sets to interpret the audio channels incorrectly as a result of spurious noise on their sound demodulator outputs.

The TDA9840, TDA9845 and TDA9847 all feature the same stereo/dual sound identification circuitry and differ only in their external control mechanism and analog signal processing. The TDA9840 provides level adjustment, stereo balance control and signal source switching for I^{2}C-bus controlled TVs and VCRs, the TDA9845 provides simple logic level control of signal switching in low-cost VCRs and the TDA9847 provides complex main/auxiliary input switching for TVs and VCRs that have SCART connector facilities. All three sound processors require few external components and can be used with a fixed pilot frequency bandpass filter so that the circuit becomes completely alignment-free, simplifying the TV/VCR production process.


Use of these stereo/dual sound processor ICs eliminates any tendency for TVs or VCRs to interpret audio channels incorrectly.

The on-chip digital phase-locked loop, referenced to an external 10 MHz crystal, generates a synchronized pilot carrier which is used for synchronous demodulation of the identification signals. The stereo and dual sound identification tone demodulators feature very narrow bandwidths of ±1 Hz to ensure extremely reliable identification, while the bandwidth of the pilot carrier detector is deliberately greater than ±50 Hz so that it can track pilot frequency variations from the transmitter if synchronization with the video's horizontal lines frequency is temporarily lost. A Schmitt trigger threshold detector in front of the digital identification PLLs also helps prevent spurious noise on the inputs from causing incorrect identification.

Reader Service 182

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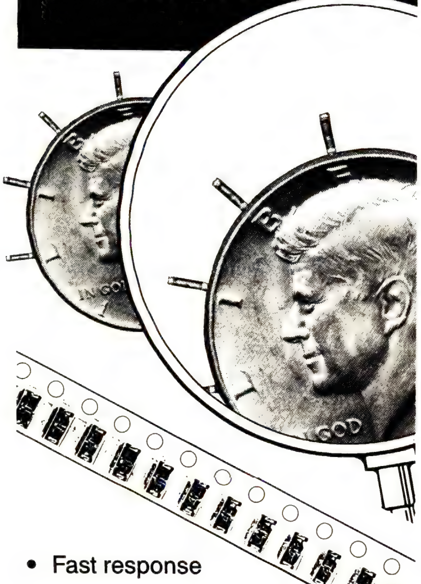

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READER SERVICE 170

TECHNOLOGY BRIEFING

RESHAPING USER INTERFACES

My favorite user interface is my car's, whose dashboard gauges are mostly analog. I can quickly see current and optimal levels in speed, fuel level, and engine temperature. The shape of the instrument display matters, too. Curiously, the speedometer on some new car models is designed as a semicircle—with 130 mph on the right and 70 mph at center. Two flaws in the design are that 130 mph is hardly realistic: On New Jersey's crowded highways, the rare occasion to hit maximum speed would surely draw a state trooper's attention; the 55-to-65-mph range is too compressed and too far left of the main line of sight.

The importance of user interfaces carries over to electronic design, where their design is receiving more attention these days. That's none too soon as is pointed out in *Set Phasers on Stun and other True Tales of Design, Technology, and Human Error*. In this 1993 book, Steven Casey describes how failures in user interface design had fatal consequences in nuclear power and chemical plant accidents, medical treatments, and plane crashes.

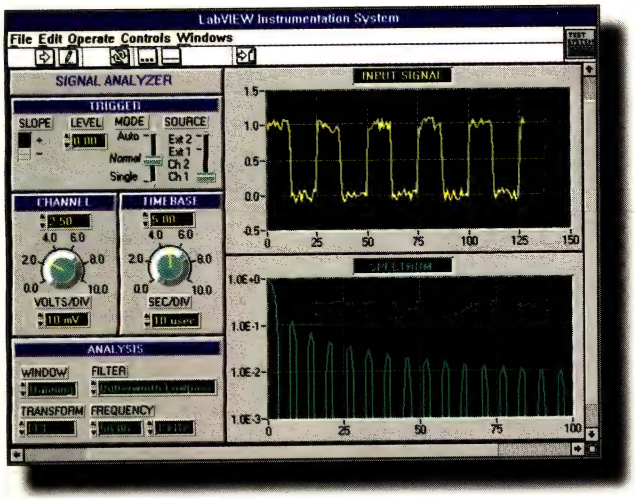
SHERRIE VAN TYLE
SOFTWARE EDITOR

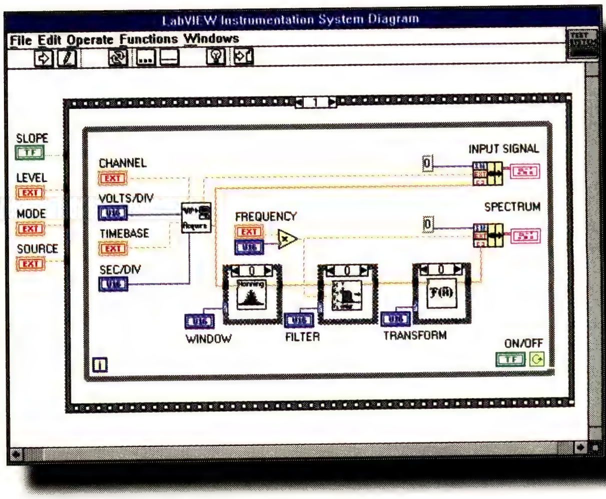
Consider process control, where animated graphical displays of data on desktop PCs and workstations are replacing the hardwired gauges and dials for monitoring and controlling data in aerospace, defense, telecommunications, and other areas. To develop these displays, developers have created dynamic GUI toolkits for writing custom displays that monitor and control many real-time applications. For these software tools to be useful, though, advances were made in interactive control of monitored processes; desktop computing horsepower also has kept pace. As a result, a new industry has grown up around interface development technology. For instance, the market for real-time data visualization tools, which amounted to 5000 development licenses last year, is expected to hit 25,000 licenses by 1996, according to the X Business Group, a Fremont, Calif., market research group for X and graphic interface tools.

Development of animated GUIs still has plenty of challenges. The availability of development tools is offset by the fact that developers must create proprietary interfaces for end users of vertical applications in telecommunications, petrochemical applications, and so forth. Moreover, GUI development tools aren't standardized across platforms. Because the interface code is part of the application software, changing the GUI means grappling with the source code. Fortunately, tool vendors are filling these development gaps with products like DataViews, SL-GMS, Sammi, and VAPS. For Unix, for example, the latest version of Data Views, 9.5, complies with Motif's widget, or object, programming model so that X/Motif developers can integrate animated graphics into Motif interfaces. With the point-and-click drawing editor, engineers can draw visual representations of their process control environments, such as tanks, valves, planes, or vehicles. By eliminating the complex coding that goes into creating these animations, development time is trimmed by up to 80%.

Other promising links in the development chain are Windows NT and Chicago, to which products such as Data Views will eventually be ported. Assuming developers get some help with complex APIs (application programming interfaces), porting development tools to advanced environments may free developers from tedious implementation details, giving them more time to create effective, intuitive animated interfaces. For instance, ten years ago, in Bhopal, India, the Union Carbide Corp. plant's control room gauges showed pounds per square inch gauge (psig), but there was no historical trace to show operators the rapid, and disastrous, rise in pressure of methyl isocyanate within the holding tank. Compared with a needle on a dial that must be read, an animated display of a tank that's bulging or changing colors gets an operator's attention, quickly overcoming barriers of language, education, and skill level.

More than Just Ease of Use ...





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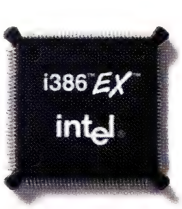
READER SERVICE 128

Introducing the fi
for embedd



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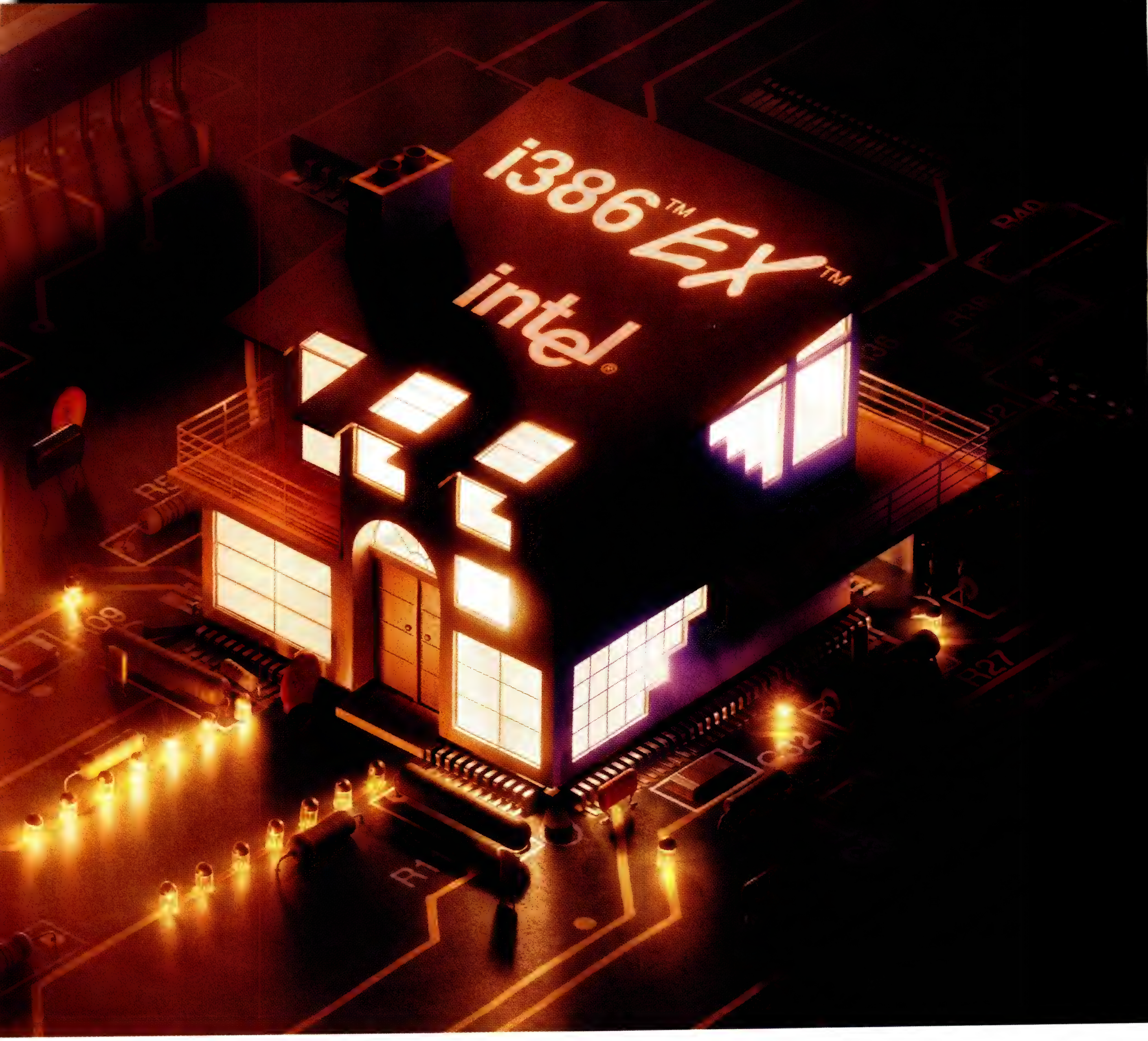

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couldn't be easier. The off-the-shelf tools and support of the PC architecture will allow you to get your designs out more quickly, and differentiate them with familiar interfaces like DOS and Windows*.

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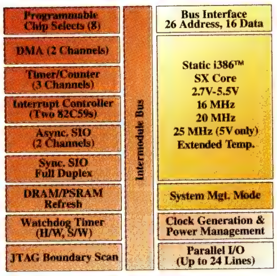
Embedded Intel386™ EX Processor Block Diagram


Programmable Chip Selects (8)
DMA (2 Channels)
Timer/Counter (3 Channels)
Interrupt Controller (Two 82C59s)
Async. SIO (2 Channels)
Sync. SIO Full Duplex
DRAM/PSRAM Refresh
Watchdog Timer (H/W, S/W)
JTAG Boundary Scan
Intermodule Bus
Bus Interface 26 Address, 16 Data
Static i386™ SX Core 2.7V-5.5V 16 MHz 20 MHz 25 MHz (5V only) Extended Temp.
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Higher integration, lower cost. The higher density of 4-Mbit VRAMs reduces chip count for more efficient use of board space and increased system reliability. The dual asynchronous data ports simplify the CPU interface and greatly reduce the memory bandwidth bottleneck. Add that to our Total Integration™ philosophy and it equals cost-effective designs.

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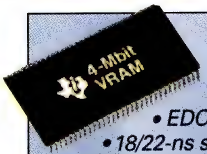

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READER SERVICE 146

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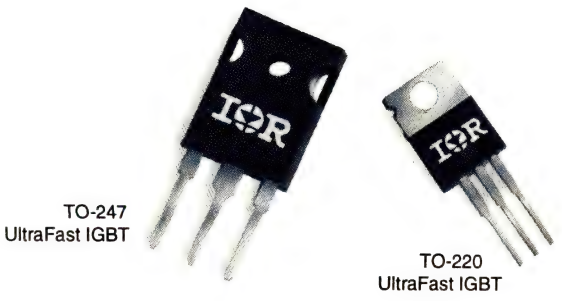

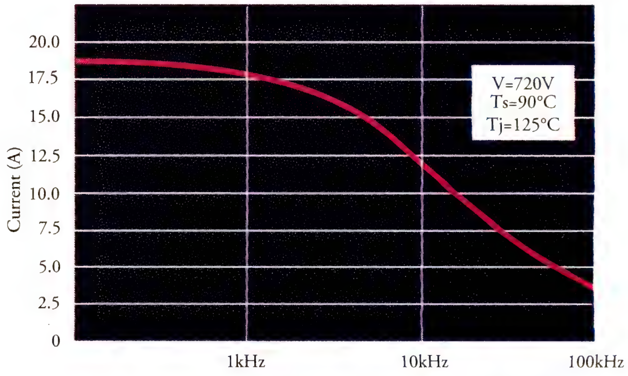

Output current vs frequency for two IRGPH50KD2 in half-bridge, 50% duty cycle.

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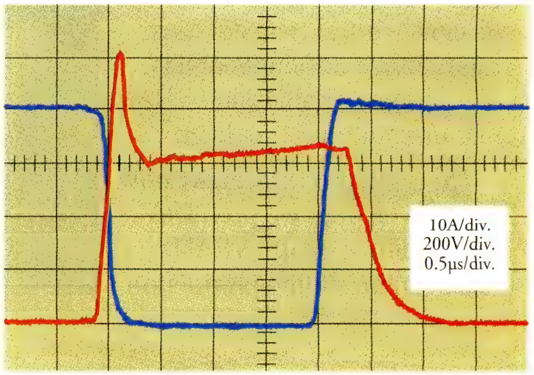

Switching waveforms of the IRGPH50KD2 in a clamped inductive load at Tj = 90°C.

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READER SERVICE 176

TECHNOLOGY NEWSLETTER

COMMUNICATIONS INDUSTRY EYES MPEG1/MPEG2

Efforts are underway by the X303.1 committee of the Computer and Business Equipment Manufacturing Association (CBEMA), on behalf of the American National Standards Institute (ANSI), to define the requirements of a set of communications interface standards, MPEG1/MPEG2. Heavily driven by the broadcast industry, the committees' requirements will formulate the U.S. position on these standards. This information then will be presented to the International Standards Organization (ISO), Geneva, Switzerland, toward the development of an international standard.

The MPEG1 (Motion Pictures Expert Group) standard, currently being introduced in trials for cable and direct-broadcast TV, operates in the 1.2- to 1.5-Mbyte/s range, and is directed toward CD-ROM and PC applications. All changes made to this standard will be implemented into the final internationally accepted standard, MPEG2. MPEG2 will operate within the 4- to 10-Mbyte/s range, and will be fully backward-compatible with MPEG1. The standard will be used in various applications, ranging from ATM and the communication or storage of video to just about anything pertaining to the information superhighway. Information regarding the MPEG1/MPEG2 standards, including comprehensive analysis and design information, will be presented at a seminar on August 26 in Santa Clara, Calif. Detailed descriptions of the standards, as well as trade-offs and implementation information, will be discussed. For more information, contact Kristine Kneib at (619) 459-8058. *CA*

KNOWN-GOOD-DIE PROGRAM GETS ARPA PUSH

The ongoing effort to establish the underpinnings for the multichip-module market gained a boost when the Advanced Research Projects Agency increased its support for known-good-die (KGD) development efforts. The Microelectronics and Computer Technology Corp. (MCC), Austin, Texas, received an additional $2.3 million in ARPA funding for Phase II of its KGD project. The project is designed to ensure the availability and quality of bare die for MCMs. In Phase II, MCC will evaluate the most promising commercially available carrier technologies for KGD. A technology-assessment study will survey 30 domestic technologies, taking note of technical capabilities, readiness, cost, and process impact. Phase II is being managed by the Solid State Electronics Directorate, Wright Laboratory, Air Force Materiel Command, Wright-Patterson AFB, Ohio. For information, contact Guy Couturier at (513) 255-8667. *DM*

DEVELOPMENT TARGETS SMART BATTERIES

A cooperative effort is underway to develop products that simplify charging and fuel-gauging rechargeable batteries for applications such as portable computers and cellular telephones. Energizer Power Systems, Gainesville, Fla., and National Semiconductor Corp., Santa Clara, Calif., are producing a line of batteries that Energizer will market as its Power Management brand. By placing intelligence inside the batteries, two key benefits result. For one, a smart battery can control its own charging process, thereby effectively eliminating overcharging. For another, fuel gauging allows users to better monitor the level of charge remaining in the batteries at any given time. The Energizer/NSC announcement follows on the heels of the announcement by Duracell International Inc., Bethel, Conn., and Intel Architecture Labs, Beaverton, Ore., concerning the development of specifications for standardized smart rechargeable batteries (ELECTRONIC DESIGN, *June 13, p. 50)*. For more information, contact Energizer at (904) 462-3911. *DM*

PROGRESS CONTINUES ON API SPECIFICATION

The Call Level Interface (CLI) specification, a third-generation application programming interface (3GL API) for C and COBOL, is currently in the preliminary stages of the specification adoption process. Initially developed by the SQL Access Group, Manchester, N.H., to define the set of calls for interfacing to SQL implementations, the specification now is being incorporated by a number of companies, including Apple, Borland, IBM, Microsoft, Novell, and WordPerfect, into their own technologies. The specification is based on a descriptor approach, similar to the use of descriptions already defined on the standard SQL92, which allows flexibility and the option for later extensions. In addition, the specification provides for an interface that's compatible with higher levels of the SQL standards, such as SQL92 Intermediate and Full. For more information, contact the SQL Access Group at (603) 434-0802. *CA*

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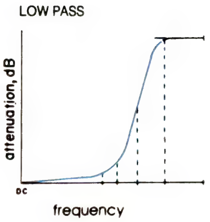


low pass, Plug-in, dc to 1200MHz

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
★LP-5	DC-5	8-10	10-200
★LP-10.7	DC-11	19-24	24-200
★LP-21.4	DC-22	32-41	41-200
★LP-30	DC-32	47-61	61-200
★LP-50	DC-48	70-90	90-200
★LP-70	DC-60	90-117	117-300
★P-90	DC-81	121-137	167-400
★LP-100	DC-98	146-189	189-400
★LP-150	DC-140	210-300	300-600
★LP-200	DC-190	290-390	390-800

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
★LP-250	DC-225	320-400	400-1200
★LP-300	DC-270	410-550	550-1200
★LP-450	DC-400	580-750	750-1800
★LP-550	DC-520	750-920	920-2000
★LP-600	DC-680	840-1120	1120-2000
★LP-750	DC-700	1000-1300	1300-2000
★LP-800	DC-720	1080-1400	1400-2000
★LP-850	DC-760	1100-1400	1400-2000
★LP-1000	DC-900	1340-1750	1750-2000
★LP-1200	DC-1000	1620-2100	2100-2500

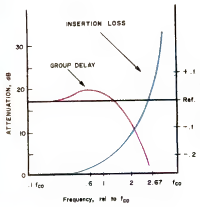
Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

Surface-mount, dc to 570MHz

SCLF-21.4	DC-22	32-41	41-200
SCLF-30	DC-30	47-61	61-200
SCLF-45	DC-45	70-90	90-200
SCLF-135	DC-135	210-300	300-600

SCLF-190	DC-190	290-390	390-800
SCLF-380	DC-380	580-750	750-1800
SCLF-420	DC-420	750-920	920-2000

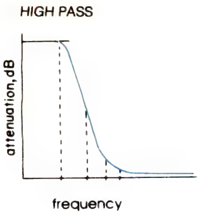
Price, (1-9 qty), all models: $11.45



Flat Time Delay, dc to 1870MHz

Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	Stopband MHz loss > 20dB	VSWR Freq. Range, DC thru 0.2fco X̄	VSWR Freq. Range, DC thru 0.6fco X̄	Group Delay Variations, ns Freq. Range, DC thru fco X̄	Group Delay Variations, ns Freq. Range, DC thru 2fco X̄	Group Delay Variations, ns Freq. Range, DC thru 2.67fco X̄
★BLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
★BLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
★BLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
★BLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
★BLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
★BLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

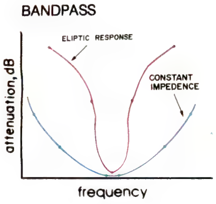


high pass, Plug-in, 27.5 to 2200MHz

Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband, MHz loss < 1dB	VSWR Pass-band Typ.
★HP-25	DC-13	13-19	27.5-200	1.8:1
★HP-50	DC-20	20-26	41-200	1.5:1
★HP-100	DC-40	40-55	90-400	1.8:1
★HP-150	DC-70	70-95	133-600	1.8:1
★HP-175	DC-70	70-105	160-800	1.5:1
★HP-200	DC-90	90-116	185-800	1.6:1
★HP-250	DC-100	100-150	225-1200	1.3:1
★HP-300	DC-145	145-170	290-1200	1.7:1

Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband, MHz loss < 1dB	VSWR Pass-band Typ.
★HP-400	DC-210	210-290	395-1600	1.7:1
★HP-500	DC-280	280-365	500-1600	1.8:1
★HP-600	DC-350	350-440	600-1600	2.0:1
★HP-700	DC-400	400-520	700-1800	1.6:1
★HP-800	DC-445	445-570	780-2000	2.1:1
★HP-900	DC-520	520-660	910-2100	1.8:1
★HP-1000	DC-550	550-720	1000-2200	1.9:1

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95



bandpass, Elliptic Response, 10.7 to 70MHz

Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	Stopbands I.L. > 35dB at MHz
★BP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
★BP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
★BP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
★BP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
★BP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95,
BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
★IF-21.4	21.4	18-25	1.3 & 150	DC-220
★IF-30	30	25-35	1.9 & 210	DC-330
★IF-40	42	35-49	2.6 & 300	DC-400
★IF-50	50	41-58	3.1 & 350	DC-440
★IF-60	60	50-70	3.8 & 400	DC-500
★IF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in $14.95,
BNC $36.95, SMA $38.95, Type N $39.95

NOTE: ★**Add Prefix P, B, N, or S for Pin, BNC, N, or SMA connector requirement.**

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A unique surface-mount package offers a feasible solution for 1-W power applications, including dc-dc converters, telecommunications, air bags, laptop computers, and peripheral 1.8- and 3.5-in. disk drives. The SOT-223, developed by International Rectifier Corp., El Segundo, Calif., features an optimized design that combines a traditional SOIC outline with an enlarged drain connection to improve thermal performance. The 1-W power application package, which is cost-effective and saves space, currently isn't available for existing products. With its clever design, board space and package height are each cut by about 30%. The SOT-223 fits the existing industry-standard surface-mount package D-pak footprint, and accepts a die of up to 2.5-mm^2. Also, it can accommodate a wide range of individual power-MOSFET products. For further information, call Gene Sheridan at SMD Power MOSFETS at (310) 607-8978. *CA*

EFFORT UNDERWAY TO PUSH TEXT RETRIEVAL

An agreement signed by Excalibur Technologies Corp., San Diego, Calif., and IBM's Software Solutions Division (SWS), combines the efforts of the two companies to provide consumers with a powerful text-retrieval product. The product, SearchManager, incorporates a leading technology of text fuzzy search, developed by Excalibur, known as Text Retrieval Server (TRS). TRS technology is based on an adaptive pattern-recognition processing engine that maximizes precision, recall, and relevancy in applications requiring free-form, intuitive queries to retrieve information. In addition, the technology uses an application programmer's interface (API) to provide multiuser network-wide access to data, and enables content-based indexing, recognition, and retrieval of text data in client/server environments. Implementation of this technology with the SearchManager product, available for workstations running on the AIX and OS/2 operating systems, will quickly and reliably allow consumers to find the information they need, when they need it. For more information on the text-retrieval product, contact Darrell Atkin of Excalibur Technologies at (619) 625-7900. *CA*

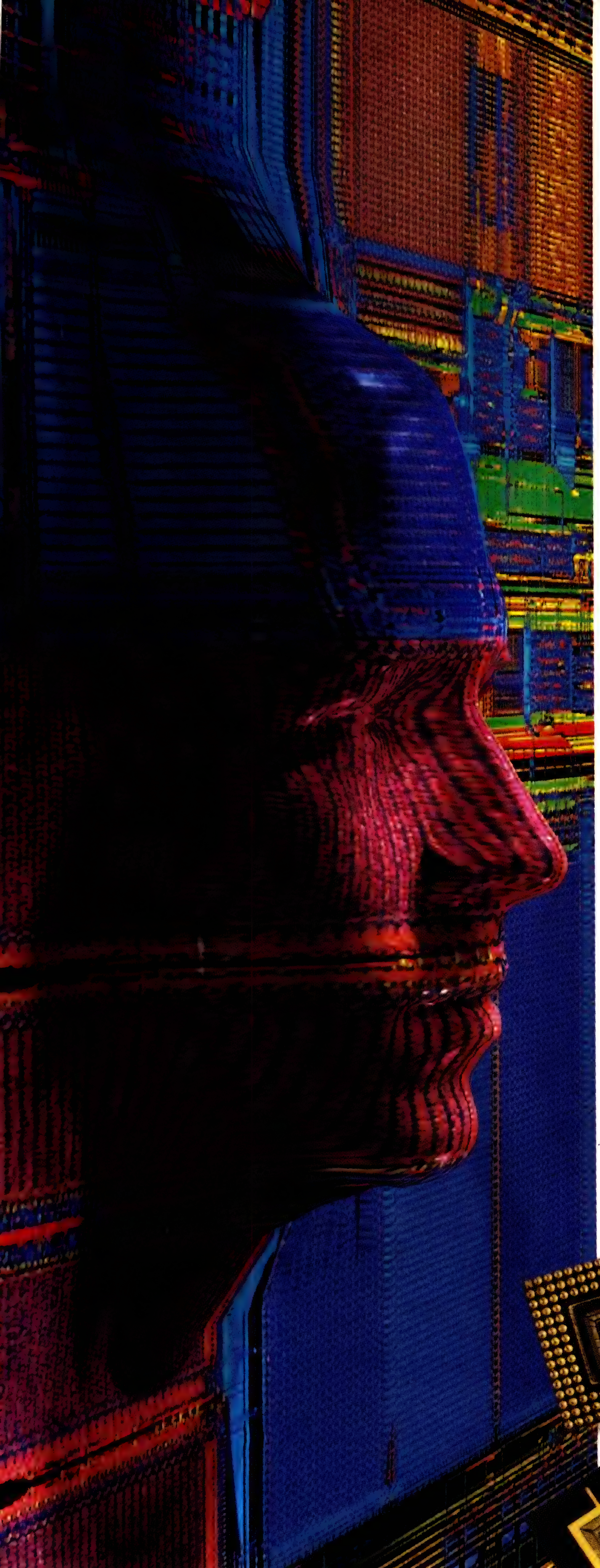
SPEC PUTS ADD-IN BOARDS IN NOTEBOOKS

A new specification is underway that would standardize a form factor for add-in cards. As a result, those cards could be used in both notebook and desktop computers. The Small Form Factor (SFF) specification calls for boards to measure 54 mm wide by 85.6 mm long by 3.3 to 10.5 mm high. It supports 32-bit operation with a migration path to 64 bits. Making all add-in boards the same size will remove a burden from both end users and board developers. Users can buy one board and interchange it between systems. Developers will only have to design one form factor, regardless of the board's destination. In addition, some of the steam is taken out of PCMCIA-based designs. The SFF boards can be built more cost-effectively than PCMCIA cards with similar functionality because some of the strict packaging and connector restrictions are removed. The SFF specification, which is being touted by IBM and Western Digital, among others, has already been adopted by the PCI committee. *RN*

EDA, SILICON VENDORS ADDRESS MODEL ISSUES

A group of EDA, semiconductor, and model companies are joining forces to address issues surrounding the availability of digital-simulation models. Diversity of group membership will help ensure all perspectives are covered, improving the chances for development of a standard that meets with global acceptance. The group, named Open Model Forum (OMF), met in San Jose in mid-May and chartered itself with increasing the availability of simulation models by defining an open procedural interface between models and simulators. The interface will enable model interoperability while protecting all parties' intellectual property.

OMF plans to zero in on current issues, such as time-to-market, reducing the complexity and cost of porting models, and improving customers' ability to upgrade simulation capability without sacrificing the use of existing models. Work will begin with the determination of the requirements, processes, and costs associated with creating the standard. Costs will be divided equally among the members. The ad hoc executive committee currently includes representatives from Cadence, IBM, Intel, Mentor Graphics, Motorola, Synopsys, and Texas Instruments. Steve Sherwood of Mentor Graphics is the group's chairman. The OMF encourages any interested end-equipment designers to attend the group's meeting. The next meeting will take place in mid-August. For more information, contact OMF with an e-mail message at omf-info@cfi.org. *LM*



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SHARP

PROGRESS REPORT

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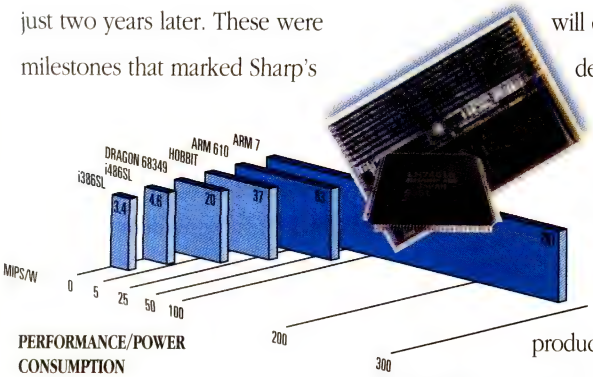

PERFORMANCE/POWER CONSUMPTION

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For example, tomorrow's global positioning, auto-routing, auto-steer, voice recognition and collision-avoidance subsystems will owe a large debt to Sharp's new 32-bit RISC processors now being produced under the ARM® partnership. Low-cost, high-performance, fully supported microprocessors like the ***LH74610*** and ***ARM7 Core*** are making 32-bit performance practical in consumer products — from games and electronic books to interactive video and voice recognition.

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By mating ARM and other microprocessors with an array of leading Sharp memory devices, you can achieve unduplicated efficiencies in data access, density and device throughput.

Recently, Sharp became the first manufacturer to offer ***8 and 16 Mb page-mode MROMs with 50 ns access times.*** That's performance comparable to the speed of EPROMs, but at *half* the price. And, to meet customers' memory-hungry but space-conscious design criteria, Sharp will also be the first to offer 64 Mb MROMs as well as 32 Mb MROMs in *both* 5-volt and 3-volt configurations.

Sharp's newest 8 Mb and 16 Mb MROM achieve their 50 ns access speeds by using a page-mode function that reads a page of information at once. Sharp offers an industry-leading 6 - 8 week turnaround time.

32-bit computing: Sharp keeps driving ahead.

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Sharp is perhaps still best known as the leader in ***active matrix and other flat panel displays.*** From personal digital assistants to the world's largest flat panel full-motion monitors, Sharp TFT displays are helping lead the evolution toward compact, portable displays of superb resolution, viewability and low power consumption.

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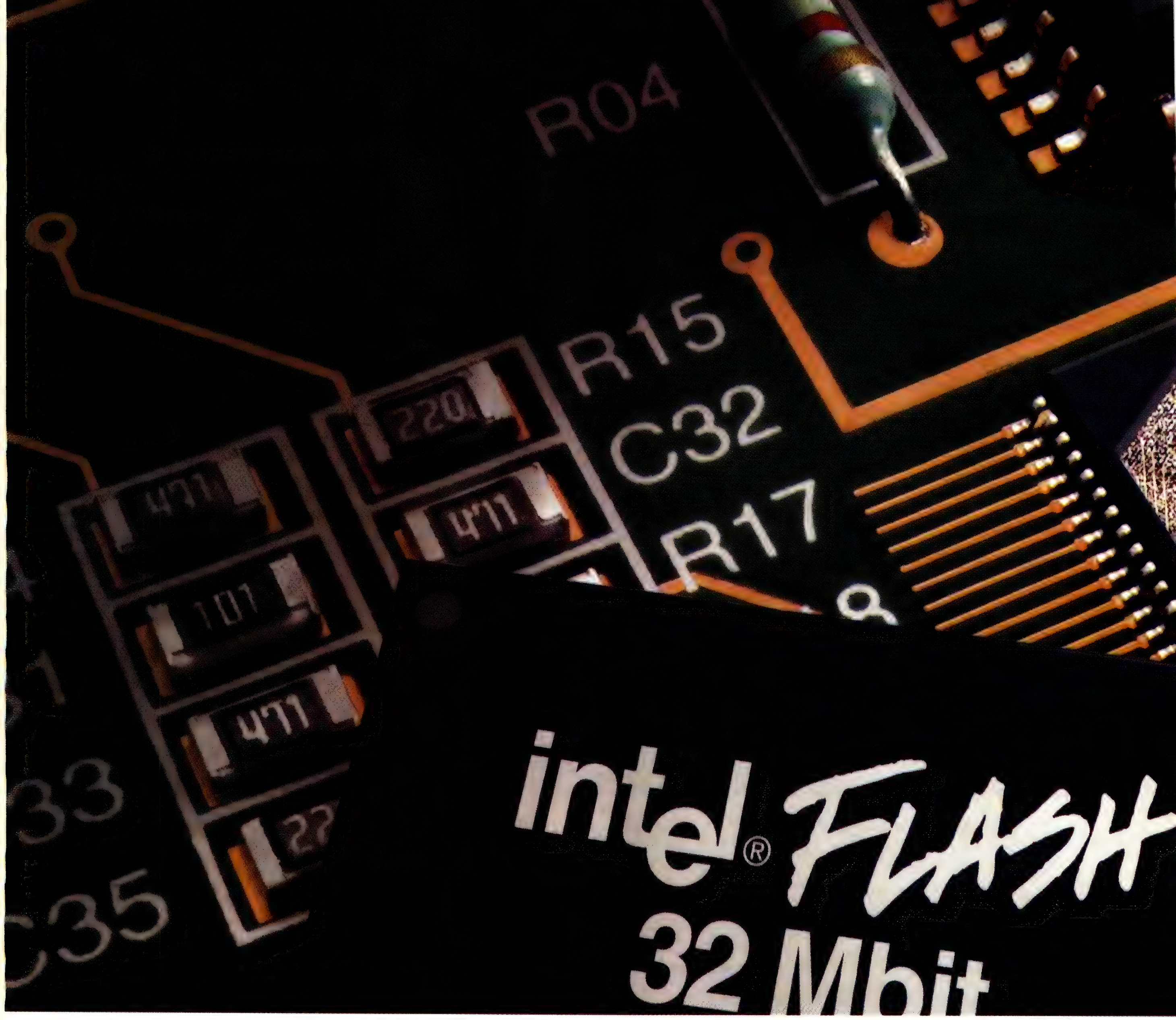

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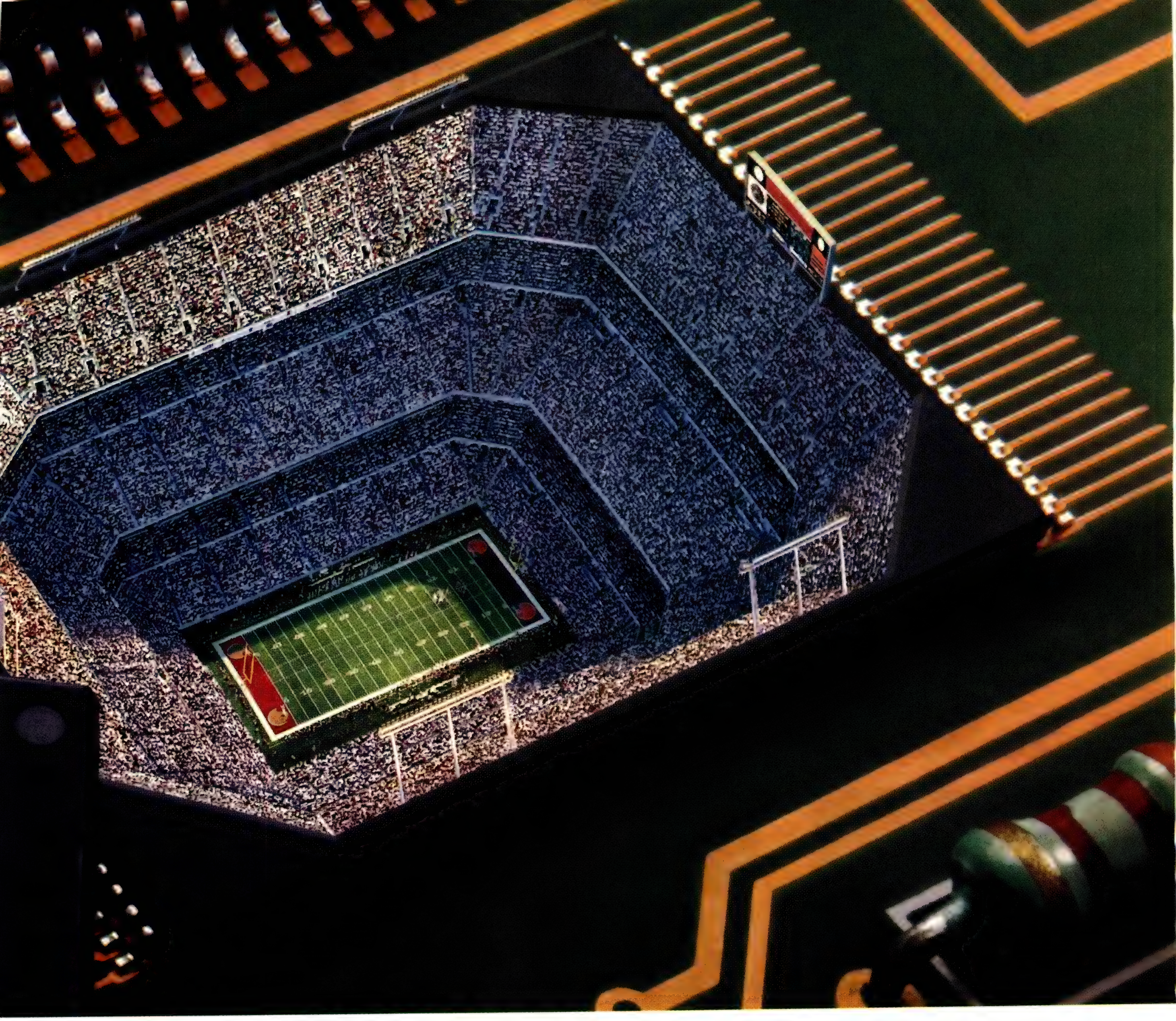

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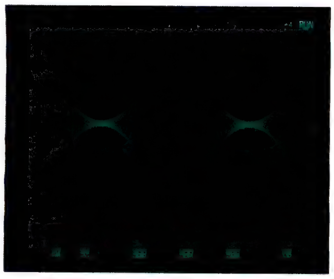

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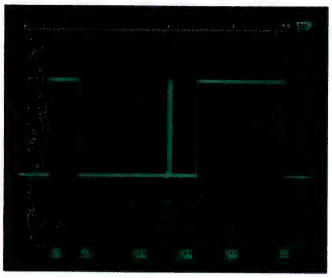

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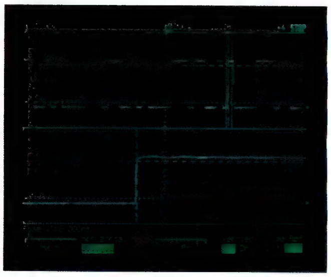

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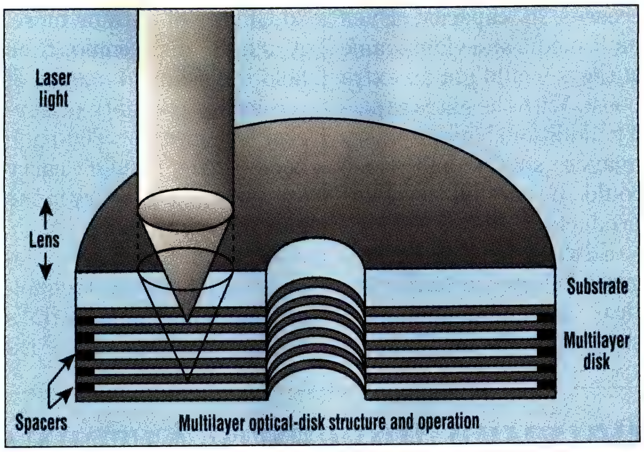

Multilayer optical-disk structure and operation

The advent of the information superhighway coupled with the latest advances in multimedia applications has made the need for access to huge amounts of data a necessary requirement rather than just a desired product feature. Compact disks have been used to hold large amounts of data, but they're no longer feasible in many applications. A single CD usually can't hold enough data to accommodate the average person's needs. Engineers traveling to various work sites with PCs may often have to take a carload of CDs along. And, the software engineer who develops computer games and wants to add audio and visual enhancements doesn't want to be limited by the data-storage capacity on a CD. Future CDs, then, not only must supply access to large amounts of data, but in a manner that's both reliable and cost-effective.

Thanks to a recent development and demonstration of a new and innovative method of storing data, such requirements now can be met by multilevel optical disks. They boast a ten-fold or more increase in optical data capacity with minimal cost increase.

Conventional CD optical data-storage systems consist of one recording surface, typically made of plastic, with a reflective aluminum coating. Information is stored in the reflective surface of the disk as circular rows of tiny bits.

To access the stored information, a laser beam, oriented perpendicularly with respect to the disk, is shone through the clear disk onto the reflective back surface. As the laser light hits the bits at the surface, fluctuations are created in the reflection of the light as it bounces off the surface. These fluctuations produce a code corresponding to the 1s and 0s of the digital computer code, which allow the disk drive's head to read the information stored on the CD platter.

This method of conventional optical data storage has provided an effective means of storing not only computer text, but audio and video information as well. However, it's quickly reaching its limit on maximum allowable data-storage capacity.

Numerous researchers have investigated various ways to increase the storage capacity of CDs, primarily focusing on increases in the density of information that could be written on one disk surface. In addition, attempts have been made to increase the storage capacity of these disks by shortening the wavelength of the laser beam's light, typically blue-light lasers, thus creating a finer focus. This method, while expected to invoke a two-fold increase in data-storage capacity, may not be large enough to meet the needs of future multimedia applications. With these increases in capacity, minimal at best, and the requirements for future data capacity continuing to rise, researchers are already hitting the proverbial brick wall.

Scientists at IBM Corp.'s Almaden Research Center, San Jose, Calif., think they have found the solution. They developed a unique design for CDs that relies on a multilevel approach. The design focuses on increasing the overall number of recording surfaces that comprise a disk, rather than the areal density of each disk. This allows for an increased data-storage capacity by as much as ten-fold or more over that available from conventional compact disks. Furthermore, the multilevel optical disks maintain the same high-quality images, sound, and video, if not better, than that currently available with conventional CDs. As a result, high-capacity storage is achieved without sacrificing traditional quality standards.

The design of the multilevel optical disk is relatively simple and straightforward, taking its basic framework from conventional CDs currently on the market. Each disk consists of individual layers of recording surfaces, typically made of plastic or glass, and separated by spacers that are glued together into a stack *(see the figure)*.

For the optical-disk drive's laser beam to be able to penetrate all layers in the stack, each layer must be virtually transparent. To this end, the aluminum coating typically found in conventional CDs isn't on the recording surfaces in a multilevel disk.

With minor adjustments to the optical-disk drive, the absence of this coating becomes negligible and a high level of signal-to-noise quality is maintained. Data can be stored on any one of the surfaces in the stack.

To read or write data, the lens in the optical-disk drive moves up and down, and its laser light focuses on an individual surface. Crosstalk between layers isn't a problem thanks to the sharp focusing mechanisms found in today's optical-disk drives. In fact, with the laser light focused on an individual layer being 10,000 to 100,000 times more intense than that hitting any adjacent layer, the interference from adjacent disk surfaces is virtually non-existent.

While it's technically possible to produce multilevel disks that offer both read and write capabilities, a read-only disk requires only minor disk-drive modifications, while a disk with write capabilities requires substantially more complex modifications. In addition, the writing process requires that the disk materials absorb some of the laser light, reducing the transparency of each layer.

Although these obstacles make it more difficult to produce write-once multilevel disks, they're not insurmountable. To date, scientists have demonstrated 2- and 4-layer write-once disks that can be written on and read from, as well as 2-, 4-, and 6-layer read-only disks. Future read-only and write-once multilevel disks are expected to contain more recording surface layers, with the maximum number of surfaces ultimately being limited by the power of the laser beam and the transparency of the layers in the stack.

For the first time, high-capacity increases are possible through minimal changes to the conventional compact-disk design, as well as the optical-disk drive. Future optical-disk drives, which will accept both conventional compact disks or multilevel disks, will be modified to be able to differentiate between the two types. In addition, future disk drives will need to be able to recognize the numbers of recording layers in a multilevel disk and react accordingly. With the growing need for increased storage space, though, and a cost that's estimated to be very competitive, these changes could be just around the corner.

With such a large increase in capacity offered, it's no wonder that various companies are vying for the use of this technology in future applications. One market, expected to reap significant benefits, is the motion-picture industry. By using multilevel optical disks, feature-length movies could conceivably be stored as high-resolution digital video on a single CD platter. Multi-disk optical libraries, or jukeboxes, also will experience dramatic increases in capacity. Even multimedia and video-game authors would get an extra boost. With the extra capacity, additional high-quality images, sound, and video could be added to their products.

Edward M. Engler, program director of IBM's Optical Storage Laboratory, says that, "I can imagine that future multilevel disks that include other capacity increases, such as advances in areal density, could store 30 Gbytes of data or more. A single disk could then hold the scanned images of the entire contents of several thousand 200-page books. You could carry around a small library in the palm of your hand."

While a product implementing this new technology doesn't exist yet, IBM's researchers feel that it's only a matter of time before such a product is made available. By their estimates, future multilevel optical disks could be in the hands of consumers everywhere in as little as two years, and at a price that is less than two times the cost of a typical CD sold today.

For further information, contact Mike Ross at the Research Division of the IBM Almaden Research Center at (408) 927-1283.

CHERYL AJLUNI

POLYMER PRESENTS ALTERNATIVE TO EPOXY FOR PC BOARDS

A thermosetting polymer material has been developed that offers multiple technical advantages over the conventional epoxy resins widely used in the fabrication of printed-circuit boards. This new thermosetting polymer material could form the basis for an enabling technology that will impact future generations of compact, portable systems such as cellular telephones and personal digital assistants to name a few.

The material is an outgrowth of advanced composites research at IBM Research Division's T. J. Watson Research Center, Yorktown Heights, N.Y. Called CYTUF, the polymer offers a number of desireable features such as high thermal stability, excellent electrical insulation, low moisture absorption, high strength, and inherent flame retardancy. In addition, the polymer material also bonds securely to copper, a key attribute for any pc-board material.

Some of CYTUF's most attractive benefits result from its ability to resist heat. Monolithic ICs can be bonded directly to the material's surface, potentially eliminating a level of packaging and its associated cost.

In addition, the epoxies used in some conventional printed-circuit boards include a number of environmentally troublesome fire retardants that contain bromine. These additives are all unnecessary with CYTUF.

Another key benefit is the material's electrical insulation capabilities, which aid in packing chips tightly without crosstalk and other forms of interference. The material, which is up to ten times tougher than the FR-4 material commonly used to make printed-circuit boards, can be easily drilled and processed without cracking. Furthermore, Its dimensional stability and low water absorption add to its reliability.

The IBM research, led by Dr. Jeffrey C. Hedrick, focused on a group of compounds based on cyanate-ester chemistry. Although these compounds promised performance that improved on epoxy resins, their brittleness made them impractical. Attempts to drill and produce some printed-circuit boards made from these otherwise attractive materials made them crack and splinter.

Dr. Hedrick came up with an additive that toughens the cyanate by forming microscopic "islands," which intercept cracks and prevent them from spreading through the material once initiated. It took Hedrick and his team six months to iron out the additive, a thermoplastic modifier. Equally important was ensuring that the material could be manufactured with the same technology used to make epoxy-resin printed-circuit boards.

Aside from applications in multichip-module laminates, CYTUF may have applications in other areas. These include airborne antennas, satellite dishes, and other uses where the qualities of high strength and light weight are critical.

For more information about the new thermosetting polymer material, contact IBM's Dr. Gerald Present via fax at (914) 784-7650.

DAVID MALINIAK

CE is the key

Electromagnetic compatibility

Deadline January 1, 1996. After that date, all products marketed in Europe must bear the CE conformity mark, awarded only after stringent tests. And manufacturers bear liability for their products. So with the quantity and quality of electromagnetic compatibility testing on the increase, the CE conformity mark is more than just a seal of quality. It's the key to economic success on the European market.

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CONTINUOUS-SPEECH RECOGNITION BANKS ON STOCHASTIC MODELS AND SPEAKER DEPENDENCE

Speaker-independent continuous-speech recognition generally seems relegated to the fantasy world, being glorified in science-fiction movies and television programs. Now, however, many companies are trying to turn fantasy into reality.

Past efforts have yielded systems that handle small vocabularies with speaker-independent and isolated-word features (distinct pauses between words). More practical systems, though, must use speaker-dependent algorithms if the vocabularies are to grow when handling day-to-day activities.

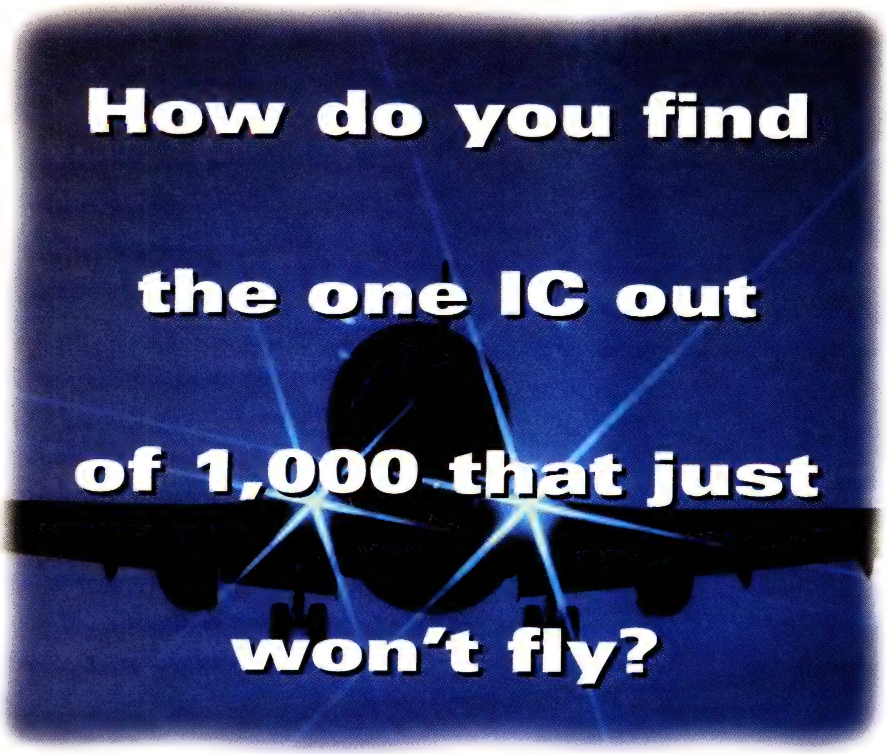
Focusing on speaker-dependent continuous-speech recognition, researchers at the Philips Research Laboratories, Eindhoven, the Netherlands, and Philips Dictation Systems, Vienna, Austria, think they have finally tuned their algorithms and hardware to deliver a speaker-dependent continuous-speech recognition system that can handle vocabularies as large as about 50,000 words.

Such a system, in addition to command and control applications, offers the promise for direct speech-to-text transcription, which ultimately could eliminate many hours of minimal productivity in the office. Note taking, report generation, and many other tasks could be totally automated, freeing time for more productive tasks.

Philips researchers, relying on its years of experience with dictation systems, created a stochastic recognition model that uses sequences of three words to perform matching and context sensing. This ensures that the correct word is selected from a group of similar sounding words (for example, "two" versus "to").

The speech is first analyzed and compared with phonemes and pronunciation libraries and matched with a language model before the recognized word sequence is delivered *(see the figure)*. Already being tested in Austria with radiologists, the system's software runs about 20% slower than real time—for each minute of speech, about 1.2 minutes is needed to analyze the speech and convert it to text. Although the initial system was optimized for the German language, Philips is developing both British and American English versions for the U.K. and U.S. markets.

In these languages, between 40 and 50 phonemes are needed. First, the speech-recognition software must decide where a phoneme or a word starts and where it ends. In continuous speech, however,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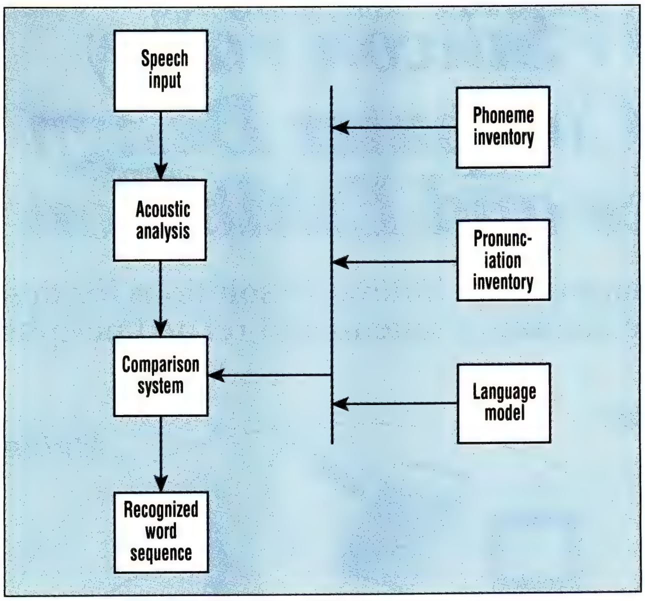
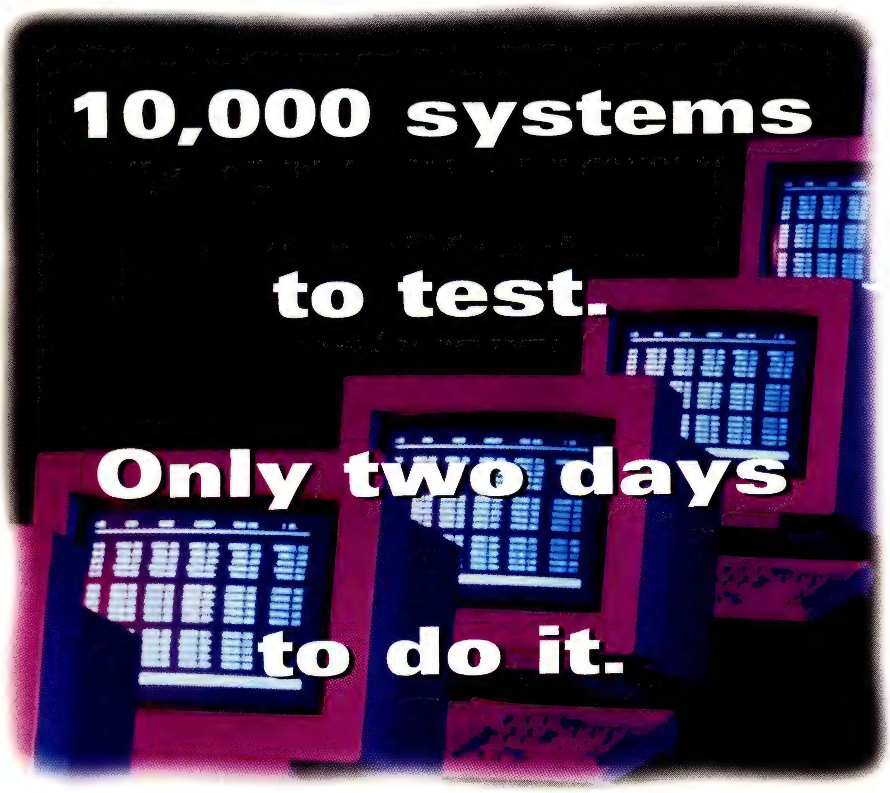
there are no anchor points such as distinct pauses with which to deduce the starting or end points. The software instead must find them by comparing the sounds to a large number of known word samples to extract and match the phonemes. Thus, building up the lexicon (vocabulary) is an important aspect of any useful system.



The stochastic language model is key to developing the usable recognition system. In the model, a collection of probabilities is established for likelihoods that one word follows another. Without such a model, the probability that one word follows another is the same for every word in the lexicon. If the choice can't be minimized, the search time required by the algorithm would be much too long and would require that the size of the lexicon be reduced to shorten the search time. The years of experience by Philips Dictation Systems not only played an important role in building the lexicon for the system, but also in determining the probabilities for one word following another.

In the past, the processing horsepower to implement continuous speech recognition has required mainframe or dedicated computer systems. That's changing, though, as both general-purpose and dedicated DSP chips are available to provide computational throughputs of hundreds of millions of instructions per second. Now, the processing circuits, coupled with improvements in algorithms, let the speech-recognition capability reside on one add-in card for a personal computer and provide working vocabularies of 50,000 or more words.

The SpeechMagic system developed by Philips is centered around a 24-bit digital signal processor—a 40-MHz Motorola 56002—and several field-programma-



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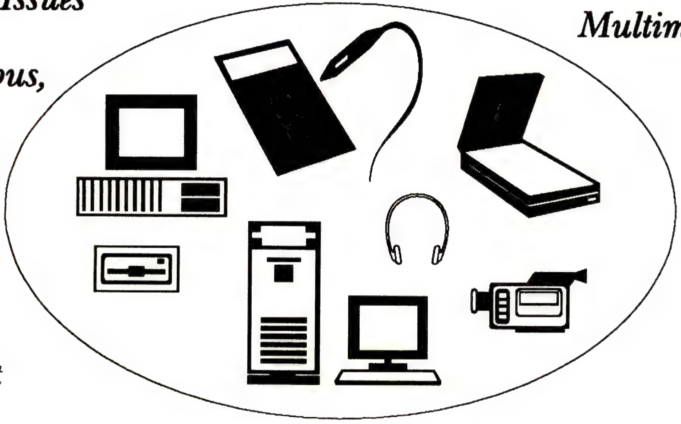

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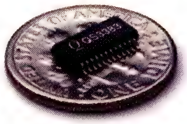

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ble gate arrays and programmable-logic chips to form an add-in card for IBM-compatible personal computers with an AT-bus . The card, which can run speech-recognition algorithms on a lexicon of about 50,000 words, has an overall throughput of about 600 MIPS. Supporting the recognition card is a speech preprocessor card that's also 56002-based, but performs the input speech capture and digitization (using PCM 256 or LPC-BB algorithms).

Fourier transforms are executed by the card on the speech by first dividing the speech into 25-ms frames. Each frame provides vector information about the recorded speech signals. That information, in turn, is used by the algorithms to extract the energy information in the speech signal as a function of frequency. A 10-ms overlap between frames helps smooth the spectrum. The energy information is then used by the recognition algorithms to match the phonemes to the lexicon.

The algorithms executed by the hardware also must take into account differences in the duration of phonemes. For example, during training, the time duration of a phoneme might be about 50 ms, while during dictation, slow speakers might stretch the phoneme to 80 ms. However, the algorithm must still recognize the phoneme. To do that, the algorithms incorporate hidden Markov Models to provide some time compression-decompression matching.

Once the phonemes are determined, the SpeechMagic algorithms use the phonemes to start searches though the lexicons. The vocabulary is set up as a binary tree so that the search will lead to individual words, to which the language information is added. The language information, in turn, is stored as a stochastic language model, which provides information on the likelihood of the recognized words appearing in the recognized sequence. Restrictions are derived from syntactic, semantic, and pragmatic sources. However, to recognize word combinations that for one reason or another don't appear in the texts used to teach the system, the probability factor is set so that it never equals zero.

Certain functions, called macros, can be assigned to handle special cases, such as times and dates or punctuation marks. These macros, once the base words are recognized, convert the text into specific forms or place a specific symbol in the text rather than the word (quote marks, periods, etc.).

Just developing a speech-recognition subsystem by itself, though, isn't enough to support office-automation applications. As a result, researchers at Philips came up with SpeechPro, which is a much more complete solution that includes development tools to create new lexicons.

Furthermore, such a recognition system doesn't stand alone, but must link in with word processors for the tasks offinal adjustments and stylization. Consequently, Philips ported the tools and the links to the Microsoft Windows 3.1 operating environment and included a DDE interface to the popular Word for Windows and WordPerfect word processors. Then, once the speech is converted to text, the text can be linked right into the word processor.

To make final editing and text transcription easier, the final package also will include such functions as foot-pedal control, speedup and slowdown playback without distortion, and other ease-of-use features commonly found on standard dictation playback units. Volume and tone settings, as well as selection between headphones and speakers, also are user options. Development tools include a vocabulary manager that allows new words to be added, sets up alternate spelling for similar sounding words, and offers many other features.

Beta testing of the SpeechMagic system is now underway in Austria and will soon be available in the U.S. from Philips Dictation Systems, Woodbury, N.Y. The SpeechMagic subsystem and predeveloped lexicon software will sell for about $3000. Price for the full developer's kit has yet to be set.

For more information about the technology and the beta-site testing, contact Hans van der Linde in the Vienna, Austria office at (043) 1 60101, ext. 1671, or fax inquiries to (043) 1 60233 59.

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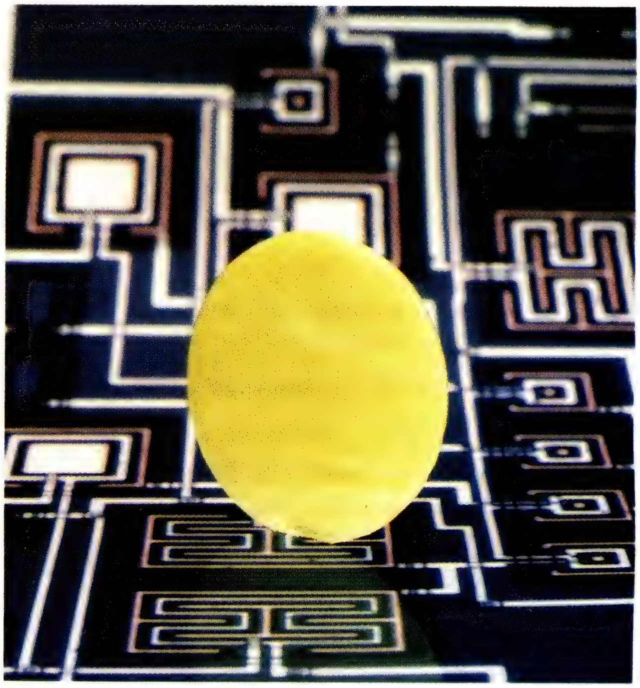

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was accomplished at the General Electric Research and Development Center, Schenectady, N.Y. *(see the photo)*. Silicon-carbide ICs are expected to be applied initially in sensors that will operate reliably in the heat generated by combustion-powered machines, ranging from automotive engines to jet engines and locomotive diesels. The sensors would monitor temperature, the degree of combustion, and other conditions. This data would be fed back to control systems that would optimize the machines' performance.

Unlike conventional sensors, those based on silicon-carbide ICs wouldn't require the extensive cooling systems that add bulk, weight, and cost to control systems. GE researchers, led by Dr. Dale M. Brown, have already designed and fabricated experimental silicon-carbide sensors that can operate at temperatures up to 350°C.

As its name implies, silicon carbide, a man-made material, is related chemically to single-crystal silicon, which is the basic building block of microelectronics. However, silicon carbide has an energy bandgap three times larger than that of silicon. This wide bandgap, which allows silicon-carbide ICs to perform exceptionally at high temperatures, also makes the material well suited for applications in blue LEDs, deep-UV photodetectors, radiation-resistant devices, and highly efficient power-conditioning devices in a wide range of power-control applications.

Silicon carbide also is superior to silicon in many other aspects. For example, it has a better breakdown field, greater thermal conductivity, and higher maximum electron-drift velocity. These properties make the material a good candidate for microwave devices used in radar and communication, very-high-speed circuits with micron and submicron geometries, and fast-recovery high-voltage diodes.

The GE research team has demonstrated that its silicon-carbide processes make it possible for any silicon foundry to fabricate circuits from the material using conventional processing equipment. For information, call Peter Van Avery at (518) 387-7574.

DAVID MALINIAK

MASSIVELY PARALLEL SUPERCOMPUTER SETS RECORD OF 143.4 DOUBLE-PRECISION GFLOPS

The world record for computing performance has been shattered, thanks to a joint effort undertaken by Sandia National Laboratories, Albuquerque, N.M., and Intel Corp., Hillsboro, Ore. The team used an Intel Paragon XP/S 140 Supercomputer to achieve a throughput of about 143.4 double-precision GFLOPS on the MP Linpack (Massively Parallel Linear Package) benchmark.

The Sandia development marks a 15% improvement over the previous record of about 124.5 GFLOPS. That record was set last August by Fujitsu's Numerical Wind Tunnel (a one-of-a-kind system owned by the-Japanese Aerospace National Laboratory).

The key element in reaching the new speed record was getting the software codes to run efficiently over all of the Paragon XP/S 140's different cabinets. The Sandia/Intel scientists accomplished this by modifying the existing Linpack code to maximize its efficiency.

The Intel Paragon XP/S 140 uses the company's own i860 XP central-processing units (CPUs). Because each cabinet has 64 slots, 64 boards (with two CPUs each) can be accommodated. This allows for a capacity of up to 128 processors per cabinet. But, due to the system's flexible configuration, some CPUs may be dedicated to the task of I/O processing, while others are dedicated to application processing.

The way Intel initially designed the supercomputer, one set of CPUs was to be used for computations, while the other set was designed for communications—there are 1840 compute processors in all. The Sandia/Intel team rewrote many of the core routines of the BLAS (Basic Linear Algebra Subroutines) Library, assembly-coded routines that provide high speeds in linear-algebra equations. This allowed them to use the communications coprocessor as a computations coprocessor instead, which ultimately resulted in the 3680 computation processors.

The data registers employed in the supercomputer system run at a speed of 64 bits/word. However, they're not considered full 64-bit CPUs because they don't support 64-bit addresses. The address structure, though, allows for 128 bits at a time with one instruction.

A top clock frequency of 50 MHz is achieved by the i860 XP CPUs. The system architecture allows for one addition operation per clock cycle, and one multiplication operation in each two clock cycles. Consequently, three operations are possible in every two clock cycles. This provides a peak speed of 75 MFLOPS with a 50-MHz clock. Employing the linear-algebra routines, however, the team was restricted to a speed of 50 MFLOPS because they had exactly one addition for every multiplication.

The new speed breakthrough begs the questions, has the Linpack code reached it's maximum utility and will a new code be needed? Not according to David Womble, senior member of the technical staff at Sandia.

"There's more that can be done to optimize the code even further," he says. "It's already close to top performance, but the performance engineers will continue to work with the code. I don't expect any more major breakthroughs, but we'll still edge ahead."

The 31-cabinet Sandia Paragon supercomputer was installed last July. It runs a hybrid operating system that combines the Sunmos operating system kernel, which was developed by Sandia and the University of New Mexico, with the Paragon operating system from Intel.

The Sandia/Intel speed record represents the third time in three years that an Intel supercomputer has held the MP Linpack title. Two Linpack records of 8.9 and 13.9 GFLOPS were set in 1991 by the Concurrent Supercomputing Consor-

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Synchronous DRAMs	16 Meg	x8	10, 12, 13	3Q94/4Q94
DRAM Modules	32MB	x32, x64, x72	60, 70	3Q94/4Q94
	16MB	x32, x64, x72	60, 70	3Q94/4Q94
	8MB	x32, x64, x72	60, 70, 80	Now
	4MB	x32	60, 70, 80	Now
88-Pin DRAM Cards and MiniCards	32MB	x32	60, 70	3Q94/4Q94
	16MB	x32	60, 70	3Q94/4Q94
	8MB	x32	70, 80	Now
	4MB	x32	70, 80	Now
SRAMs	4 Meg	x4, x8, x16	12, 15, 20, 25	3Q94/4Q94
	1Meg (revolutionary)	x4, x8, x16	15, 20, 25	Now/3Q94
	1Meg (evolutionary)	x1, x4, x8	15, 20, 25	Now
	256K	x1, x4, x8	12, 15, 20, 25	Now
Synchronous SRAMs	1 Meg	x18, x36	7, 10, 12, 15, 17	Now/3Q94
SRAM Modules	4MB	x32	15, 20, 25	4Q94/1Q95
	1MB	x32	20, 25	3Q94/4Q94
	512KB	x32	20, 25	3Q94/4Q94
	256KB	x32	15, 20, 25	Now
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tium's Intel Touchstone Delta system, which now resides at the California Institute of Technology in Pasadena.

Thanks to its speed, there are numerous potential applications for the supercomputer. For one, the machine is presently used for scientific technical computing. Intel and Microsoft recently did a technology demonstration using the scalable interconnect with Pentium boards. This allowed them to employ the computer as a video server using the MS-S Tigerfile System.

Other possible applications range from its use in a number of areas from the defense establishment to the industrial arena. For instance, weapons safety can be simulated when a shock-hydrodynamics code is used for anti-armor design. From a scientific point of view, this same code can be used to simulate the impact of the comet Shoemaker-Levy IX when it hits the planet Jupiter this summer.

In the case of industrial applications, there's a massively parallel direct-simulation Monte Carlo code (DSMC). This code is being used to simulate plasma-etching and deposition reactors designed for the integrated-circuit microelectronics industry.

For more information about the massively parallel supercomputer system, call Intel's Jon Putnam at (503) 531-5323, or Sandia's Nigel Hey at (505) 844-7015.

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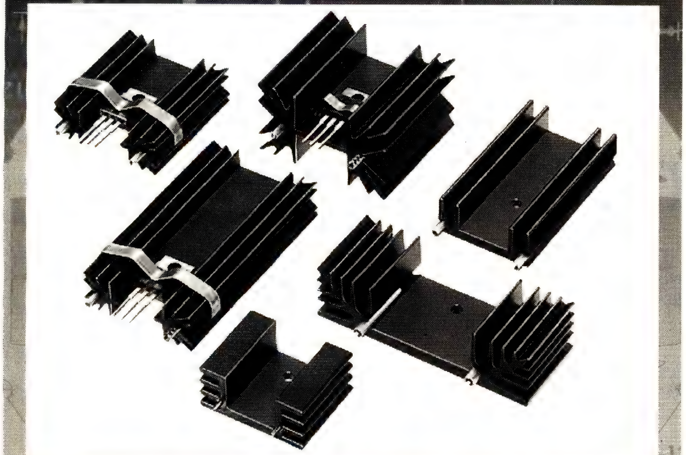

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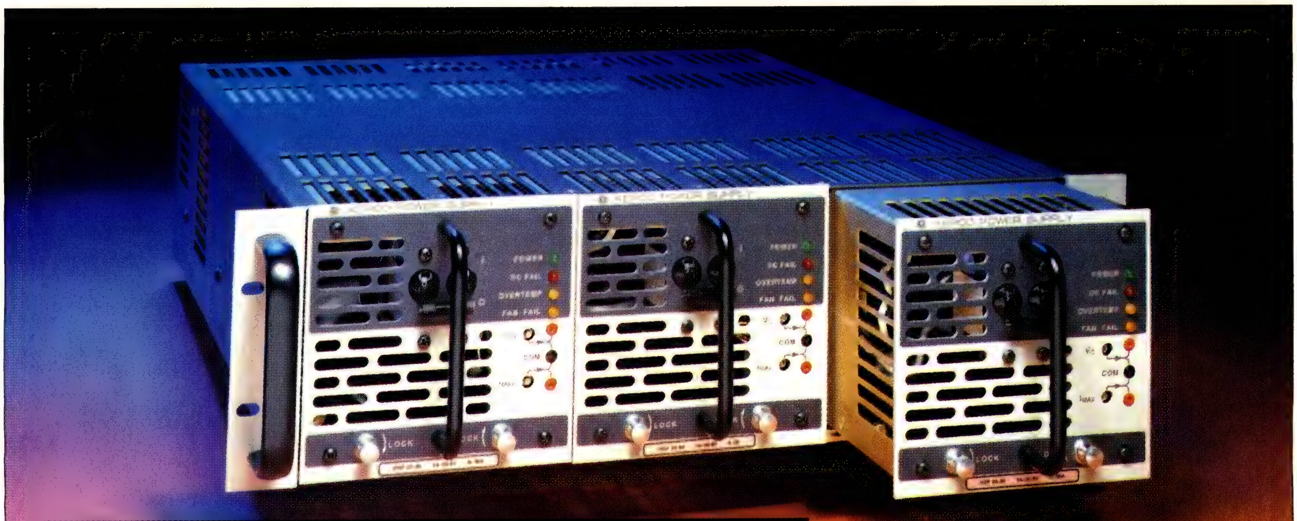

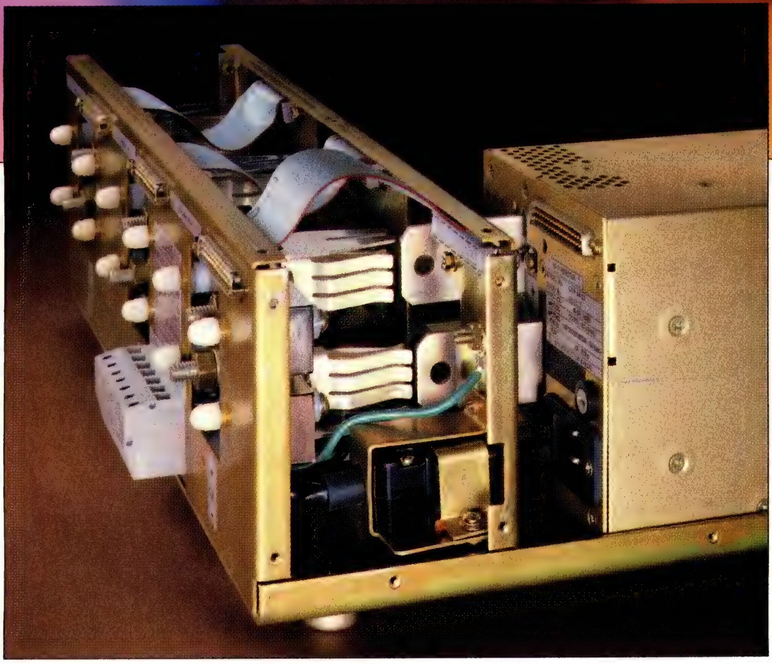

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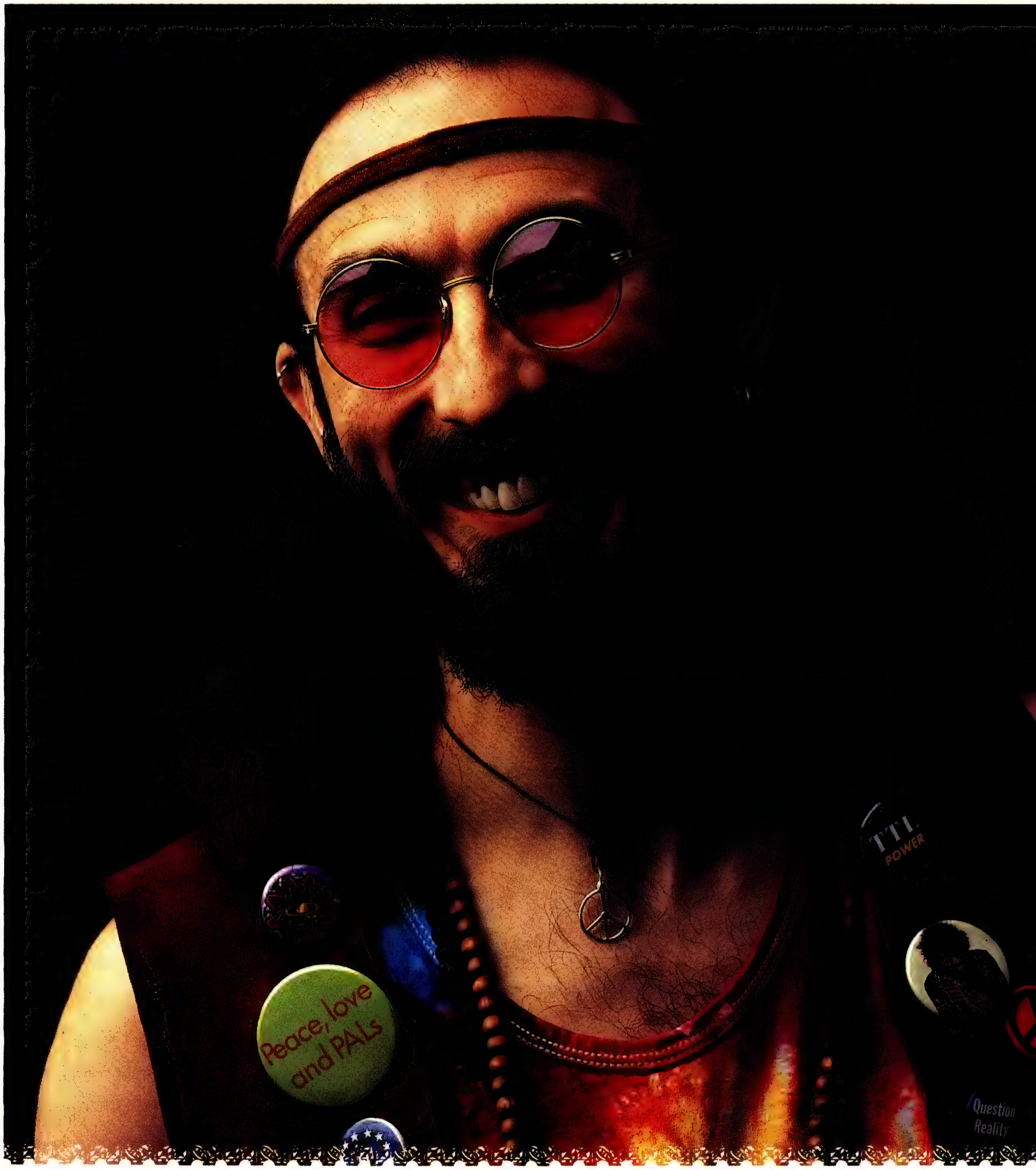

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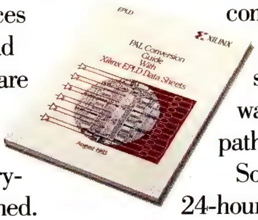

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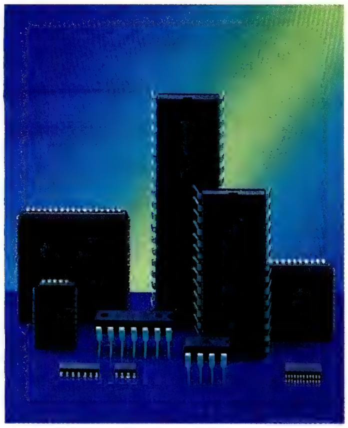

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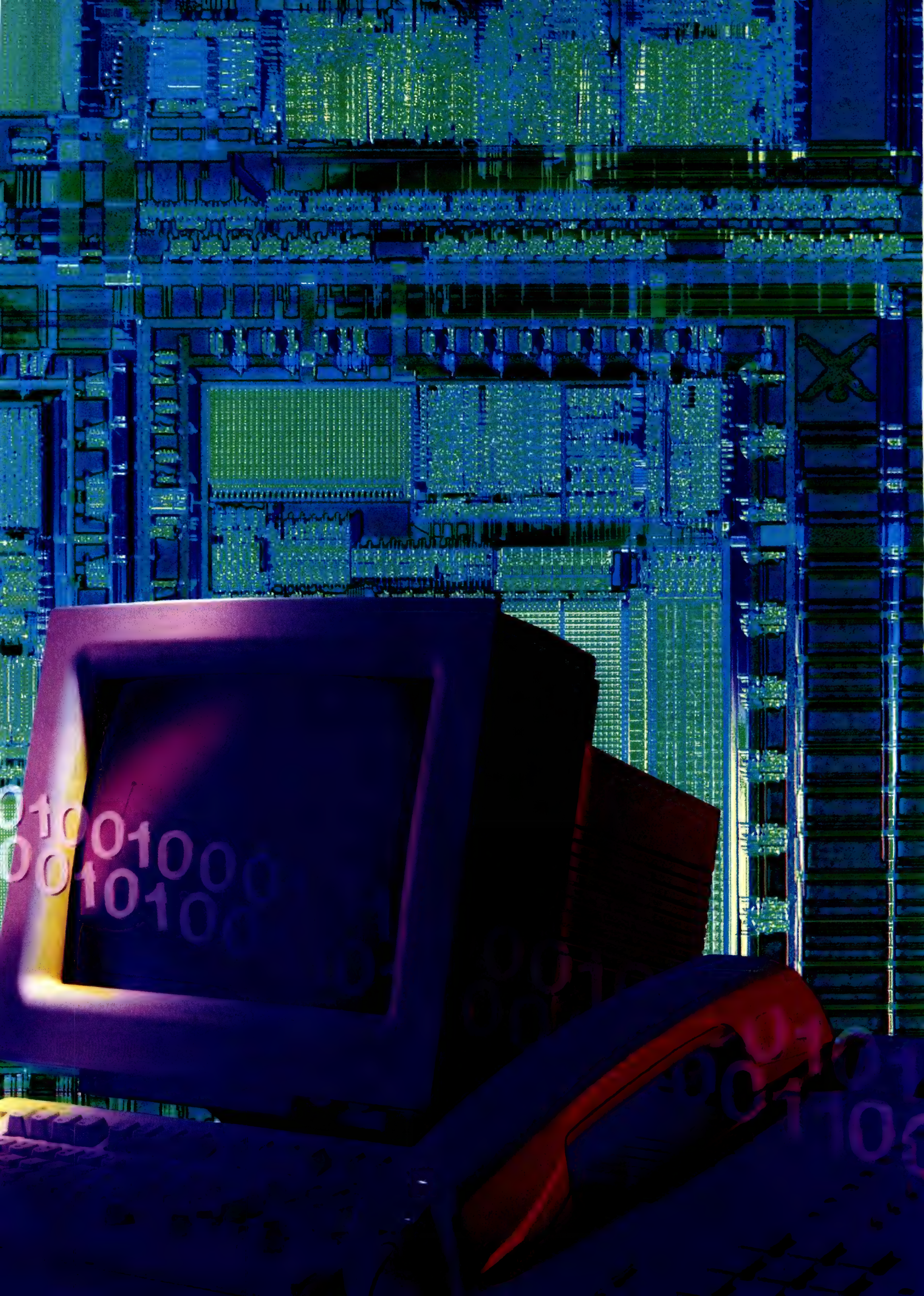
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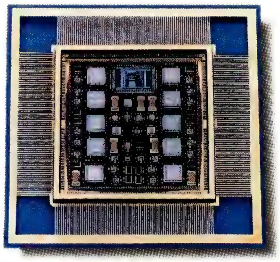

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A 0.9-V-INPUT DC-DC-CONVERTER IC RUNS 85% EFFICIENT, WHILE A COMPLETE 40-W OFF-LINE IC CONVERTER IN A TO-220 NEEDS JUST 3 PINS.

OFF-LINE AND ONE-CELL IC CONVERTERS UP EFFICIENCY

FRANK GOODENOUGH

The heightening demand for battery-powered portable systems, ranging from PCs, cellular telephones, and camcorders to medical and industrial instruments and systems, has stretched the performance of low-voltage dc-dc converters to the limit. Thus, it's essential that a battery's available energy capacity and life from the charge on a primary or secondary (rechargeable) battery are used to the maximum.

Not as obvious is the fact that these same battery-powered systems, and even some off-line systems, have put similar pressures on low-power, off-line dc-dc converters. These converters, which power portable battery chargers and are used in ac adapters, are moving inside portable PCs and even providing standby power for the so-called "green computers." They, too, must offer maximum efficiency. Moreover, both the low-voltage and off-line converters must combine minimum system cost with minimum size.

As always, when new performance demands hit the analog/power-control design community, IC designers accept the challenge and come up with unique devices. Many of these ICs employ new architectures, often patentable, with combinations of features and performance previously unavailable.

A pair of these innovative ICs, the TOPSwitch family developed by Power Integrations and the ML4890 from Micro Linear, handle maximum input voltages at opposite ends of the spectrum—700 V versus 6 V, respectively. However, despite the difference in voltage, they may often find themselves located close to each other in the same box.

The TOPSwitch converts a rectified (115 V/ 220 V) ac line into a logic-level supply rail and/or charges the battery. It also can find other applications under 150 W such as in power-factor-correcting lamp ballasts. The ML4890's task is to convert the output of a one- or two-cell battery, whose terminal voltage has dropped to 900 mV, into a rail set between 2.2 and 5.5 V that can put out 100 mA. None of these tasks are trivial. And both devices must combine minimum cost and size with maximum efficiency.

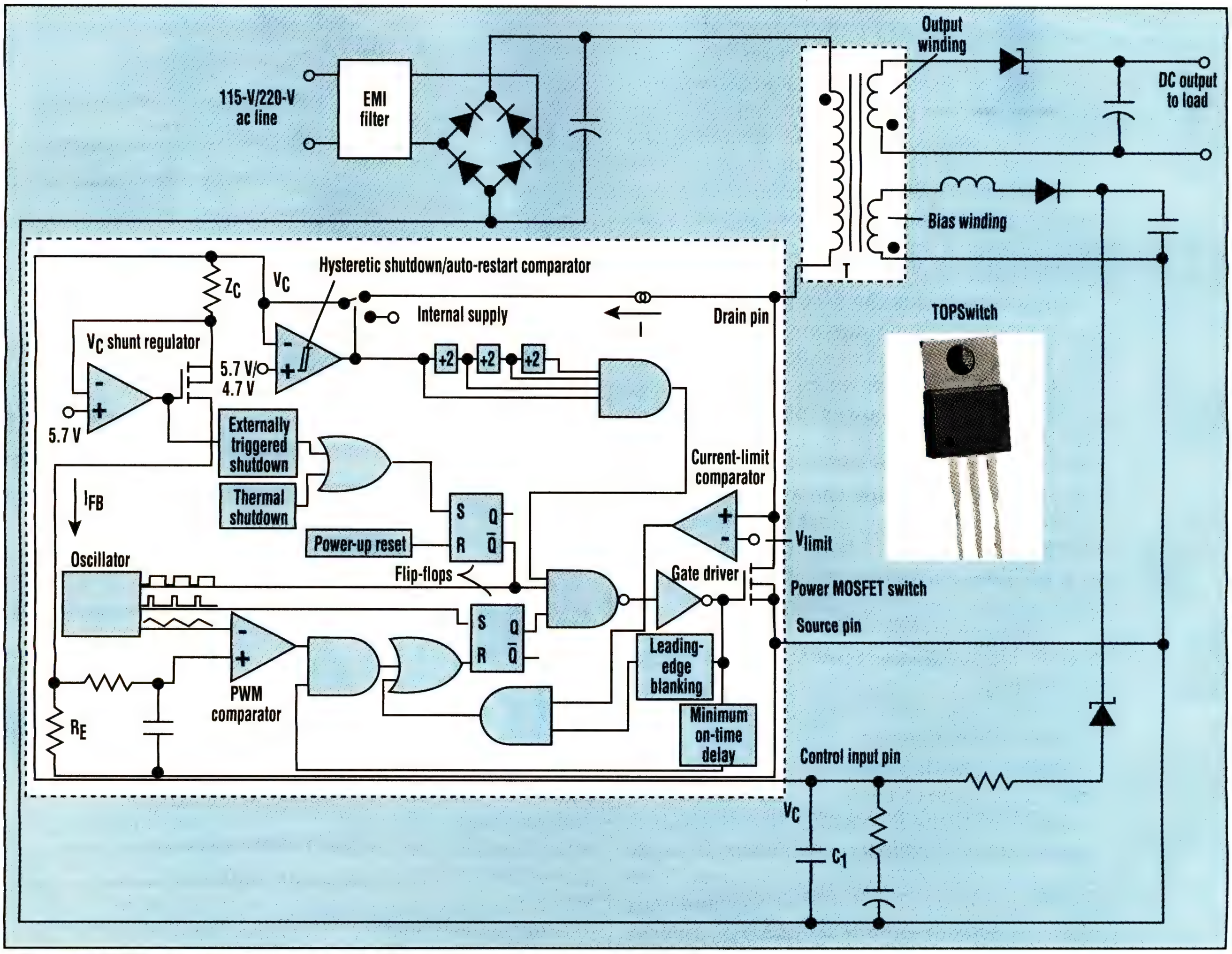
While the driving forces behind each converter are similar, they're also device-specific. For example, consumers will no longer accept an ac adapter or battery charger that's larger than and/or weighs more than their notebook or subnotebook PC, let alone use such a gross device with their pocket-sized cellular telephone or camcorder.

The smaller size not only demands a simpler circuit with fewer parts, but also greater efficiency. There's just no easy way to remove the heat from the continually shrinking package—particularly if the converter is located inside the end product (PC telephone, camcorder, etc.). On the other hand, cutting the number of batteries can further shrink the size of the end product itself, putting added pressure on size reduction for the off-line supply.

The designers of the TOPSwitch, Balu Balakrishnan and Alex Djenguerian, not only squeezed a complete (the device contains its own on-chip 350- or 700-V power switch) 40-W off-line switching regulator onto a single biCMOS die, but they also cut the pin count to just 3 by combining functions *(Fig. 1)*. As a result, this constant-frequency pulse-width-modulated (PWM) switcher comes in standard TO-220, TO-251, and TO-252 packages. The 3-pin design also reduces the total component count by 15 to 25 devices when compared with a design based on a controller and a discrete MOSFET.

In addition, the package's metal mounting surface (the TO-220's tab) is referenced to the high-voltage return of the IC's power switch. Thus, it significantly reduces common-mode EMI because the tab is at a constant voltage, rather than rapidly switching dc as high as 700 V. The 350-V versions of the IC handle the rectified 115-V ac line while the 700-V versions handle the rectified 220-V ac line and universal (115 V and 220 V) tasks. Most circuits designed specifically for 220-V jobs can develop twice the power possible from a 115-V line. That is, the chip can be used to build an 80-W/220-V power supply, but is limited to about 40 W in 115-V or universal jobs.

In the low-voltage arena, the challenge for Gordon Cook and Tim Yu was to create an IC that would permit cutting the number of batteries in a portable system from four or more to one or two, while also maximizing the total energy recovered from a battery charge (Cook came up



1. FITTING THIS OFF-LINE SWITCHING REGULATOR IC, Power Integrations' TOPSwitch, into a 3-pin package meant that the Control input pin must handle seven different tasks. These include providing chip power and negative feedback.

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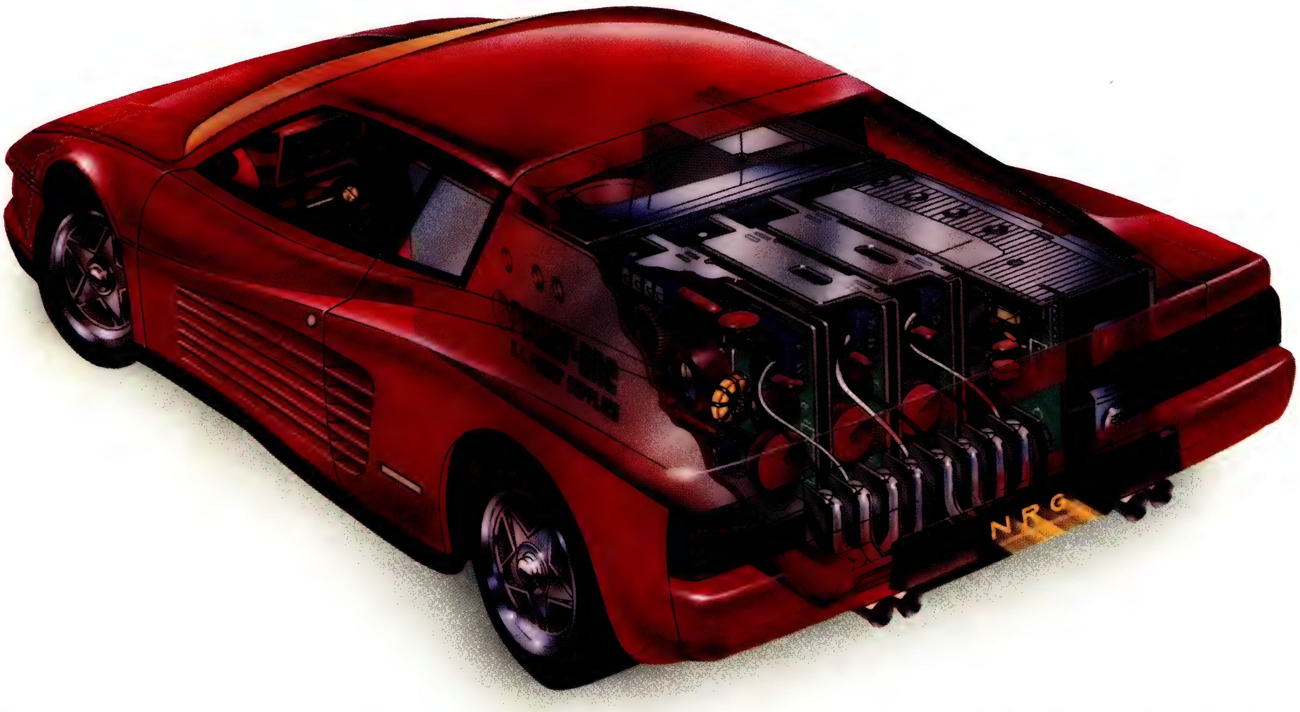

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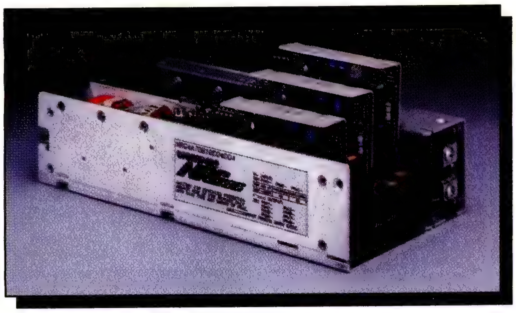

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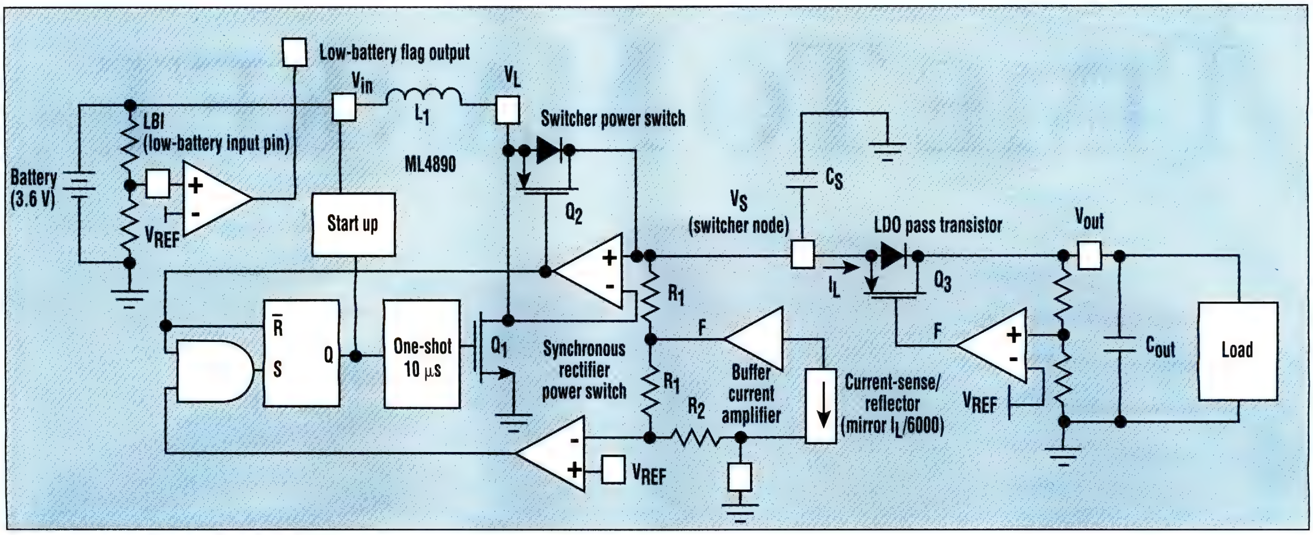

2. THIS LOW-VOLTAGE SWITCHING REGULATOR combines a boost regulator and LDO on one chip. The LDO dropout voltage in Micro Linear's ML4890 increases as load current rises.

with the ML4890's unique architecture while Yu designed the chip). They did it by adding a low-dropout linear regulator (LDO) to the output of a synchronous switching regulator *(Fig. 2)*.

Like the off-line regulator, the ML4809 is complete with two on-chip, 100-mA, 6-V CMOS switches (one switch provides synchronous rectification). This pulse-frequency-modulated (PFM) switcher operates in a "boost" topology that maximizes the battery's available energy capacity while the LDO minimizes the amount of output ripple. And all of this capability is squeezed into 8-pin SOICs and DIPs.

The problem Cook and Yu faced was critical. One of two common techniques are used today to convert a battery-pack output to a system supply rail. Either a boost-type dc-dc converter steps up the output of a lower-voltage battery or an LDO drops the output of a higher-voltage battery to the supply rail.

Boost converters are highly efficient (80% to 95%) and can get as much as 50% of the available energy capacity from the battery. But they suffer from severe ripple, which can be as much as 40 mV p-p. Alternatively, the LDO contributes no ripple and may eliminate ripple appearing on its input. However, not only is it very inefficient (on the order of 75%), but it only uses about 10% of the available energy capacity.

LDOs are inefficient because their input voltage must be higher than their output voltage. Thus, they always dissipate significant power, particularly when handling high load currents and the battery is fully charged. In addition, their available energy capacity is limited because they drop out of regulation. That is, the input voltage plus the LDO's internal voltage drop becomes lower than the output voltage demanded by the circuit's feedback loop. As a result, the LDO stops passing current and regulating its output voltage. Moreover, this dropout occurs at battery-voltages well above that at which no further energy can be obtained from the battery.

For example, using an LDO, a typical application for nickel-cadmium (NiCd) batteries requiring 100 mA from a 5-V rail (500 mW), would require five cells to obtain 6 V. A typical LDO could drop out of regulation when the input (from the batteries) drops to 5.4 V. The LDO thus only uses about 10% of the battery's available energy capacity.

A typical boost regulator, on the other hand, easily produces 5 V at 100 mA from a pair of NiCd cells (2.4 V). It can operate down to 1.2 V or even lower, utilizing 50% of the available energy capacity. Two cells not only cost less than five, but they occupy significantly less space. Moreover, a number of applications employ only one cell, impossible with an LDO alone.

At first thought, it would seem that following a boost switcher with an LDO would compound the problem, essentially multiplying the efficiencies of the two circuits and adding the reduced available energy capacity of the LDO. However, Cook came up with a unique feedback scheme that maintains a minimal voltage across the LDO's pass transistor (Q3) *(Fig. 2, again)*. In addition, putting the switcher's power MOSFET switch (Q2) and the synchronous rectifier switch (Q1) on chip with the control circuitry also upped the boost switcher's efficiency. It reduced parasitic capacitance between the control circuit and the power switches, and as lowered switch-input capacitance, reducing the losses that accrued while charging these parasitic capacitors.

In addition, using synchronous rectification (first offered by a Micro Linear PWM controller several years ago) instead of the generally used Schottky diode further increases efficiency.

The ML4890 comes in four flavors: an adjustable version in which a pair of external resistors sets the output voltage between 2.2 and 5.5 V, and a trio offering fixed outputs of 3, 3.3, and 5 V. All four also provide a Flag output that goes low when regulation can't be achieved (low battery voltage) as sensed at the Detect pin.

If the Detect pin isn't used, the

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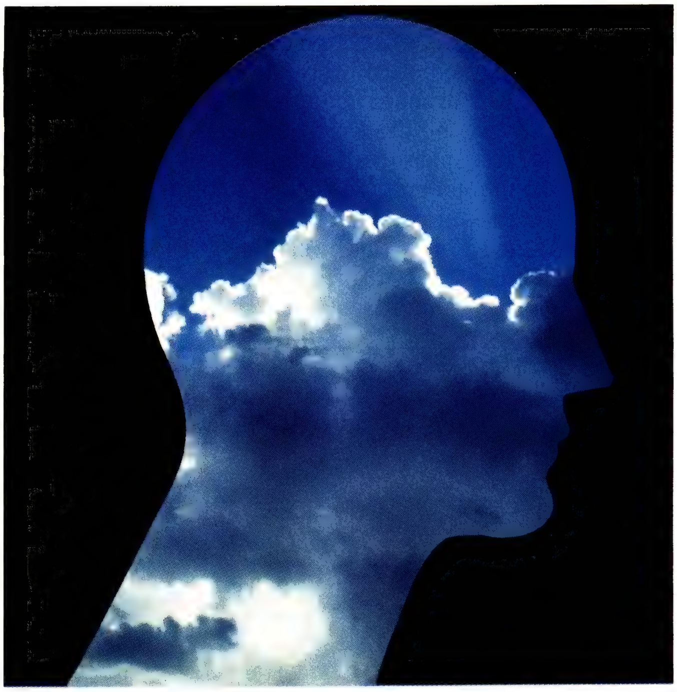

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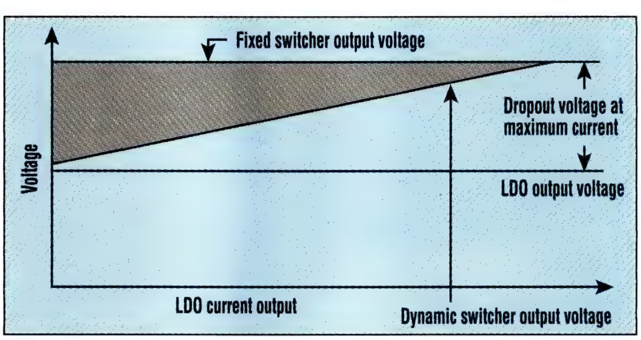
fixed-output converters need just 3 external devices: the inductor and a pair of capacitors. One capacitor, C_S, hangs on the switcher's output and its companion capacitor, C_{out}, hangs on the LDO's output. Maximum quiescent current for 20 mA of output is 100 μA, increasing to 120 μA for a 50-mA output. During startup or when shutdown occurs due to activation of the undervoltage-lockout circuit, quiescent current is 4 μA.

MIRROR, MIRROR

The ML4890's LDO provides a minimum of 30 dB of ripple rejection from dc to 200 kHz—the operating frequency range of the PFM switcher—achieving a maximum ripple of just 2 mV. Typically, available IC LDOs provide no more than 10 dB of ripple rejection between 10 kHz and 150 kHz, the frequency band in which most small switchers operate.



3. LDO EFFICIENCY on Micro Linear's ML4890 dc-dc converter is maximized by automatically raising the dropout voltage as the load current rises.

By placing the LDO on the same IC as the switcher, its patented feedback technique can maintain a minimum voltage across the LDO pass transistor *(Fig. 3)*. As the LDO's output current increases, its dropout voltage also must increase. Consequently, a switcher's typically fixed output voltage, which drives the LDO, must be high enough to provide the dropout voltage needed at maximum load current. However, because the ML4890's switcher and LDO share the same die, its circuits can sense and "reflect" LDO load current and use it to adjust the voltage across the LDO dynamically to keep operation at the most efficient level. The difference in efficiency loss between the two techniques is shown by the shaded area of the curve. The higher the load current, the higher the switcher's output-voltage level.

Three major circuits comprise the ML4890's LDO: the current sense/reflector (mirror), the current amplifier, and the feedback circuit *(Fig. 2, again)*. The current sense/reflector mirrors the current (I) in the LDO p-channel pass transistor. It scales this current down by a factor of 6000 in a patented current-mirror circuit. To respond to transient-load requirements and minimum quiescent current, the current amplifier is optimized to provide a bandwidth twice that of the switcher.

The chip's patented feedback technique continuously adjusts the LDO's dropout voltage (the voltage across the drain and source of the LDO's pass transistor Q3) to the minimum voltage needed to provide the required load current at any instant. It does this by sinking a scaled current, I/6000, from node F into buffer amplifier B. As the buffer steals current from node F, the voltage across feedback-network resistors R_1 and R_2 drops, forcing the switcher feedback node low and the switcher output voltage higher to compensate for the increased loading on the LDO.

The efficiency of the ML4890 is maximized by combining a high-efficiency, synchronous-switching PFM boost regulator with this LDO. The LDO adjusts its dropout voltage by automatically adjusting the switching frequency. This keeps the output voltage high enough to create an efficiency curve that hits 50% with approximately 200 μA of output current. Efficiency rises as the load rises to 1 mA, where it flattens out at greater than 90%. This flat curve continues until output current reaches about 80 mA, and then it begins to turn down. The LDO operates at greater than 90% efficiency over a load range of 1 to 80 mA, after which it begins to become less efficient. At 100 mA, the LDO is approximately 85% efficient.

A 500-mA and a 1-A version of the ML4890 are planned for the future to round out the family. Both versions will require the use of just three external devices and will have all power transistors on-board.

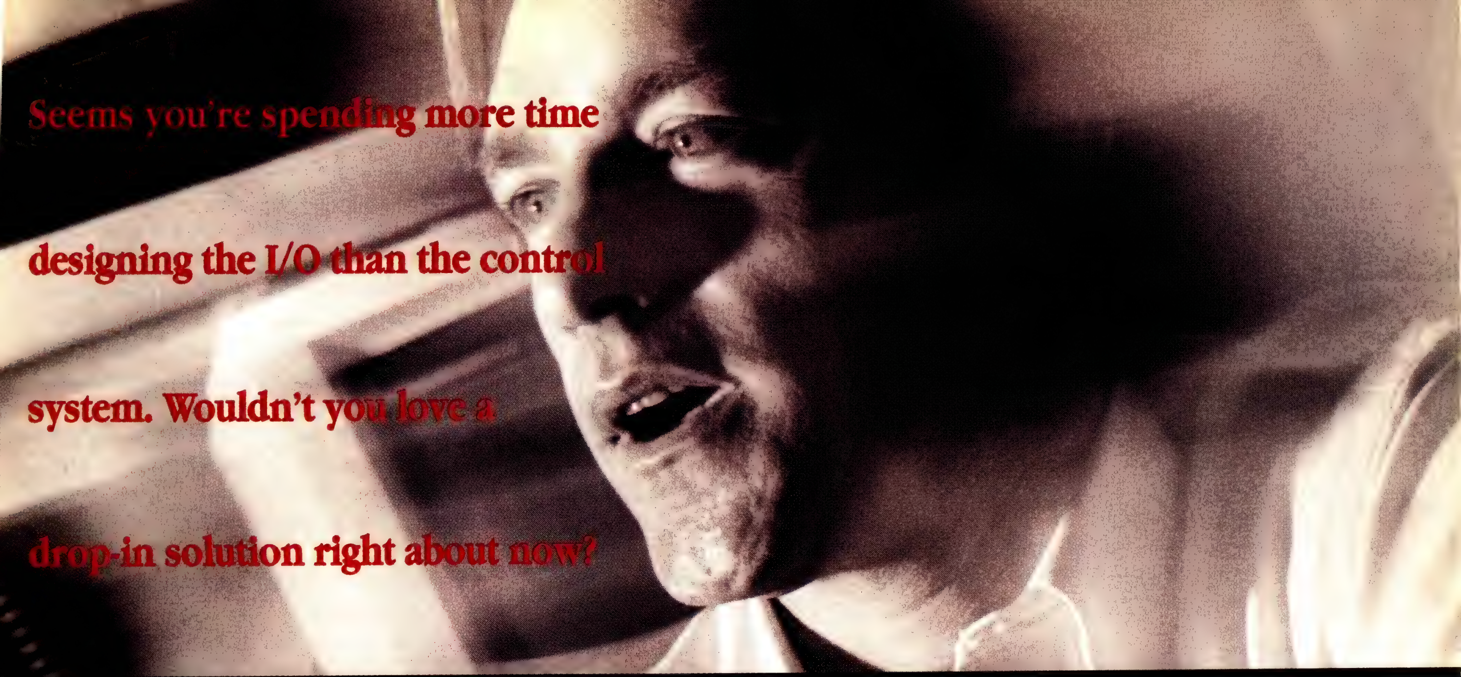
Power Integrations' TOPSwitch starts off as a large (10-member) family of converters with varied power ratings and, as noted earlier, in different packages. PWR-TOP100 series devices include 350-V switches, while PWR-TOP200 series devices include 700-V switches. Within each series, the converters differ only in the on-resistance ($R_{DS(ON)}$) of the power-MOSFET switch, and thus the current rating and the regulated power they can produce.

The 350-V PWR-TOP100/101/102/103/104 have maximum on-resistances at 25°C of 10/5/3.5/2.5/2 Ω, respectively. Built-in current-limit circuits typically limit switch currents from 700 mA for the TOP100 to 3.5 A for the TOP104. To standoff the additional voltage, the 700-V PWR-TOP200 through PWR-TOP204 have a higher $R_{DS(ON)}$, running from 18 Ω (TOP200) to 3 Ω (TOP204). Their currents typically limit at 430 mA and 2.6 A, respectively.

The ICs' high-voltage biCMOS process can build switchers to run at over 1 MHz. However, to prevent EMI, most users still want operating frequencies on the order of 100 kHz, the fixed operating frequency chosen for the TOPSwitch. In addition, the rise and fall times of the power switch were raised to 100 ns to further limit EMI without significantly raising conduction losses.

The TOPSwitch operates as a linearly-controlled current-to-duty cycle converter. During operation, the MOSFET's duty cycle decreases linearly with increasing current into the Control pin. To implement all of the control, bias, and protection functions with just 3 pins, the converter's Drain and Control pins each perform several functions *(Fig. 1, again)*.

Getting all of the TOPSwitch's functions into a 3-pin package took a number of patented breakthroughs in device structure and circuit design/topology. For starters, inte-



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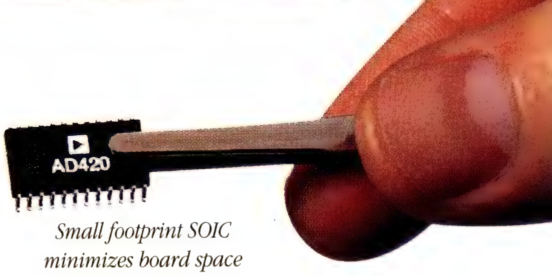

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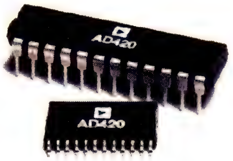

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JUST ONE PIN

Their final breakthrough came when they figured out how to get the negative feedback, compensation, and bias-supply inputs down to just one pin, the Control pin (patent #4). In addition, to make the TOPSwitch a full-featured switcher, more functions were added to the Control pin, allowing it to altogether handle a total of seven tasks:

- Providing an input for the bias-supply current.
- Offering a node on which to hang an external bypass capacitor, C_1, which supplies peak transient currents for the power-switch gate drive.
- Acting as the feedback input.
- Acting as a 5.7-V voltage-reference output.
- Providing an input for external shutdown/reset triggers.
- Supplying a node for the auto-restart timing capacitor.
- Compensating the control loop with the auto-restart capacitor used for timing.

When this PWM converter is running, the rectified output of the transformer's bias winding performs two functions via the Control input pin—power for control, and gate drive for the power switch. In addition, because gate-drive voltage V_C is a function of the converter's dc output, the converter provides negative feedback to the control circuitry.

During startup and under overload conditions, the V_C regulator operates in a hysteretic mode. During normal operation, shunt regulation separates the duty-cycle error signal (the negative feedback) from the control-circuit supply current. At startup, the V_C regulator receives power from an on-chip high-voltage current source that connects the Drain and Control pins. The current source supplies the current required to power the control circuitry and charge external bypass capacitor C_1.

At power-up, the first time V_C reaches the upper threshold (5.7 V), the high-voltage current source turns off and the PWM modulator and output transistor turn on. During normal operation (when the output voltage is regulated), feedback-control current powers the circuits running off the V_C bus. The PWM circuit creates a voltage-mode control loop by driving the output power-MOSFET switch with a duty cycle inversely proportional to the current

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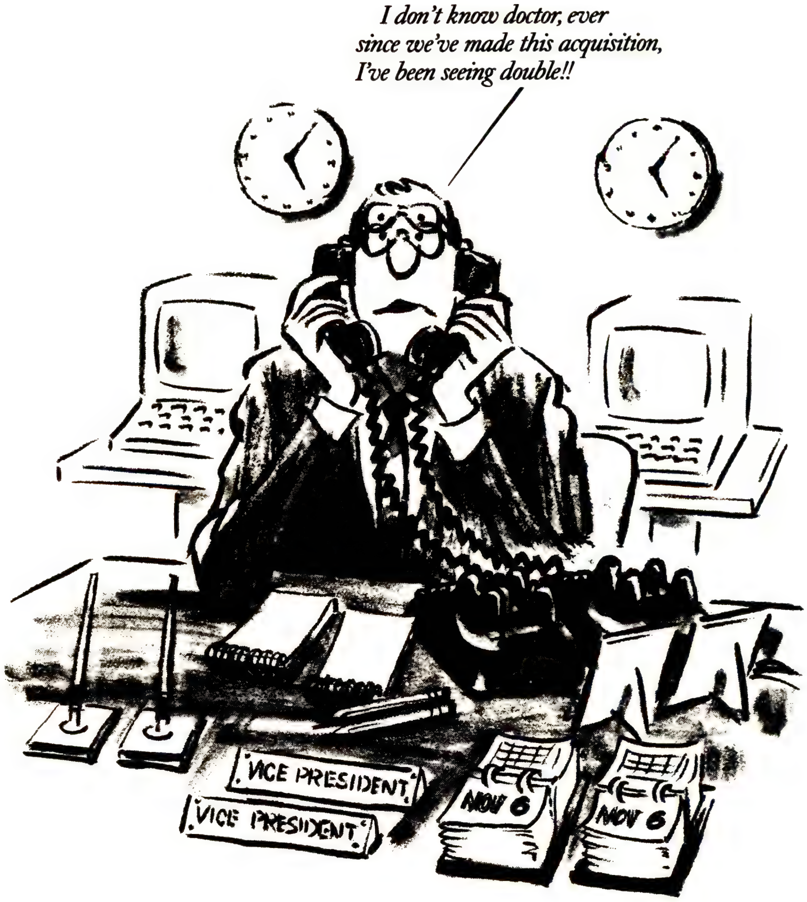
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flowing into the Control pin. The PWM comparator compares the error signal of current I_{FB} across resistor R_E with the internal oscillator sawtooth waveform to generate the variable-duty cycle waveform. Increasing control current decreases duty cycle and lowers output voltage.

FEEDBACK CURRENT

A clock pulse from the oscillator sets a latch that turns on the power MOSFET. The PWM resets the latch, turning off the output MOSFET. The duty cycle is set by the symmetry of the internal oscillator. Minimum modulator on-time keeps TOPSwitch current consumption independent of the error signal. Minimum current (typically 2.5 mA) must be driven into the Control pin before the duty cycle begins to change.

By trying to keep V_C at about 5.7 V, the shunt regulator creates the Control-pin feedback current, separating it from the minimum dc current needed to power the chip. It shunts I_{FB} through the PWM error-signal-sense resistor R_E. Dynamic impedance Z_C, connected between the control pin and the shunt-regulator FET's source, is low. Therefore, it can set the error amplifier's gain when used in a primary feedback configuration. Moreover, Z_C, together with the external resistance and capacitance on the pin (R_5 and C_6), compensates the control loop.

All critical TOPSwitch internal voltages are derived from a temperature-compensated bandgap reference. The device also generates a temperature-compensated current reference that's trimmed to set the fixed oscillator frequency and the gate-drive current for the MOSFET switch. The oscillator linearly charges and discharges an internal capacitor between two voltage levels to create a sawtooth waveform for the PWM circuit. Then the oscillator sets the PWM current-limit latch at the beginning of each cycle.

If the voltage on the Control pin's external capacitance discharges to the lower threshold (4.7 V), the output MOSFET turns off and the circuit switches to a low-current standby mode. High-voltage current source I turns on and starts to charge the external capacitance. The hysteretic auto-restart comparator keeps V_C within a window, usually between 4.7 and 5.7 V, by turning the high-voltage current source on and off. A divide-by-8 counter follows the auto-restart circuit, preventing the MOSFET from turning on until eight discharge-charge cycles have occurred. This counter effectively limits TOPSwitch power dissipation by typically reducing the auto-restart duty cycle to 5%. Auto-restart continues to cycle until output-voltage regulation is achieved again.

The chip's cycle-by-cycle, peak-drain-current-limit circuit uses the output MOSFET's on-resistance as a sense resistor. A current-limit comparator compares the MOSFET's on-

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  -EV2010 evaluation board and bq2110-KT module.
- 16-pin narrow DIP or SOIC.
- For additional data and pricing information on the bq2010 and other battery management solutions, call Benchmarq at **1-800-966-0011**.

Actual space required for implementation of bq2010 PCB.

BENCHMARQ

BENCHMARQ Microelectronics, Inc.,
2611 Westgrove, Suite 109, Carrollton, Texas 75006 U.S.A.
Tel 800-966-0011 or 214-407-0011 Fax 214-407-9845

READER SERVICE 206

state drain-source voltage with a reference. Excessive drain-source voltage due to excessive drain current turns the output MOSFET off until the next clock cycle starts.

The leading-edge blanking circuit inhibits the current-limit comparator for a short time after the output MOSFET is turned on. It prevents current spikes, which are caused by primary-side capacitances and secondary-side rectifier reverse-recovery time transients, from prematurely terminating the switching pulse.

A large current pulse into the Control pin activates the output overvoltage-protection latch. When set, the latch turns off the TOPSwitch output. A precision analog circuit turns the power switch off when its junction gets too hot (typically 145°C). Activating the power-up reset circuit by removing and restoring input power, or momentarily pulling the Control pin below the power-up reset threshold, resets the latch and allows the TOPSwitch to resume normal power-supply operation.☐

PRICE AND AVAILABILITY

The four higher on-resistance (lower-power) members of the TOPSwitch family of 350-V and 700-V off line dc-dc converters, the TOP100/101/200/201, come in TO-251 and TO-252 surface-mount D-packs. The remaining six higher-power devices, the TOP102/103/104/202/203/204, also come in the TO-220 package. Their operating junction temperature range runs from –40 to +125°C. In quantities of 10,000, the 350-V, 700-mA TOP100 goes for $1.00 each. In similar quantities, the 700-V, 2.6-A TOP204 goes for $1.92 each. Small quantities of the TOP102/103/200/202/204 will be available in June, with the remaining family members becoming available in August.

Power Integrations Inc., 411 Clyde Ave., Mountain View, CA 94043; Doyle Slack, (415) 960-3572. CIRCLE 511

All four versions of the ML4890 come in 8-pin DIPs and SOICs. They're rated over the extended commercial temperature range (–20 to +70°C), which is required for portable devices that must be used indoors and outdoors. In quantities of 1000, they go for $2.95 each. Small quantities will be available in July. Higher-current versions will be available by year's end.

Micro Linear Inc., 2092 Concourse Dr., San Jose, CA 95131; Gordon Cook, (408) 433-5200. CIRCLE 512

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MODERATELY	537
SLIGHTLY	538

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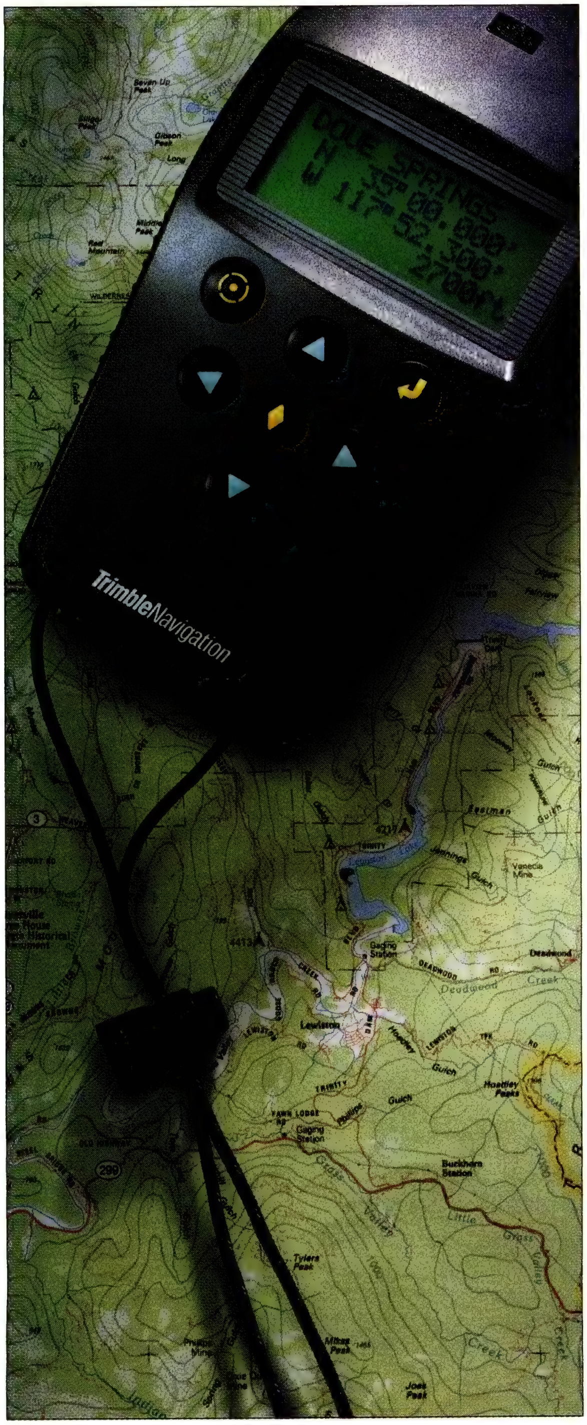

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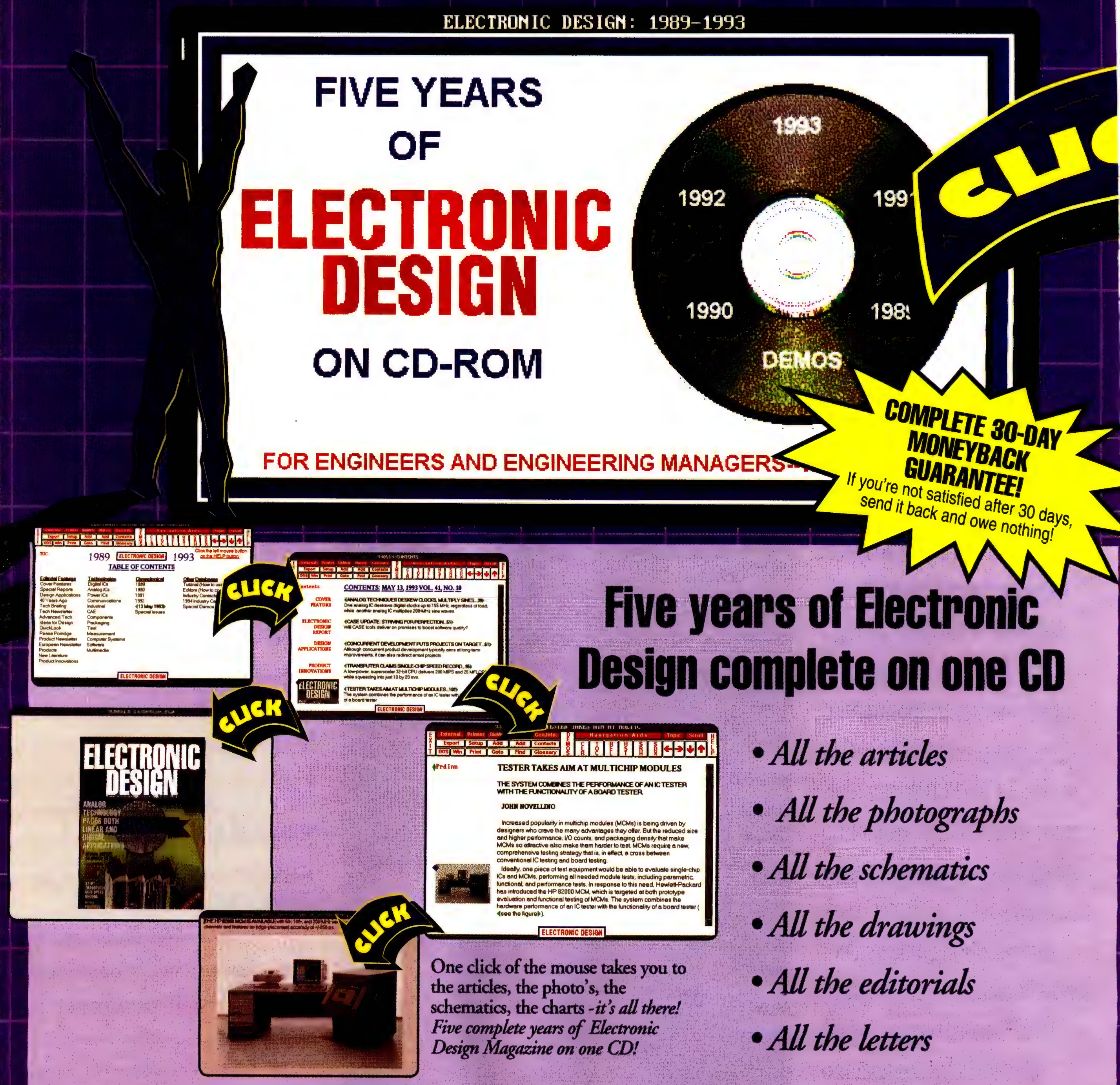

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TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER.

JOHN NOVELLINO

Increased popularity in multichip modules (MCMs) is being driven by designers who crave the many advantages they offer. But the reduced size and higher performance, I/O counts, and packaging density that make MCMs so attractive also make them harder to test. MCMs require a new, comprehensive testing strategy that is, in effect, a cross between conventional IC testing and board testing.

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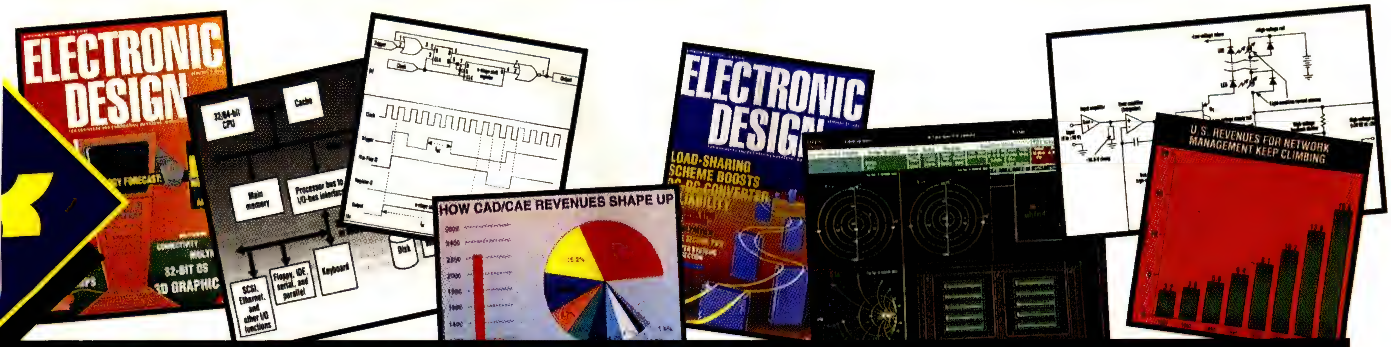
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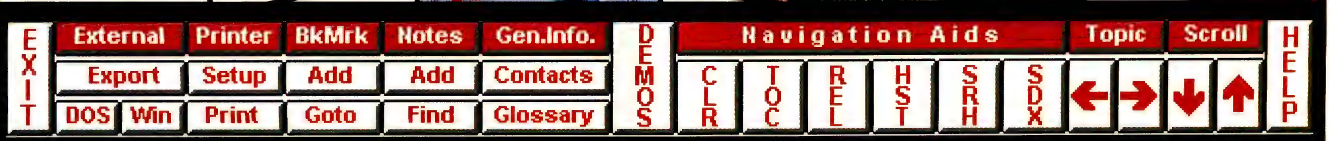

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Powerful, hypertext-based commands let you quickly and efficiently find, re-find, link, make notations, leave bookmarks, export, print, search, get product demos, and even return to your operating system!

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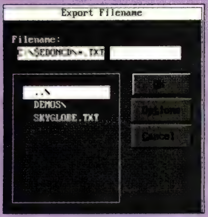
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```
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```

The **Export** button will export any or all of an article based on your selection.

DOS & Win

DOS brings you to the DOS prompt screen and **Win** takes you into Windows™ without quitting the application. These buttons make it easy for you to return to Electronic Design Magazine, where you left off, without re-launching.

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Setup & Print - This feature allows you to print articles, editorials, glossaries, illustrations, and even photos *(if your printer is capable)* directly from this CD. Great source for reference.

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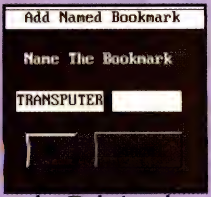
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Name The Bookmark

TRANSPUTER

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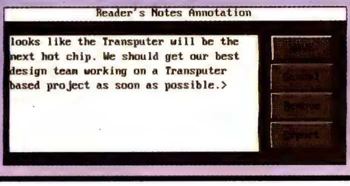

Reader's Notes Annotation

```
looks like the Transputer will be the
next hot chip. We should get our best
design team working on a Transputer
based project as soon as possible.>
```

Gen. Info - Complete reference

Contacts - Company names, addresses, contact names, phone numbers- all of the information you need to follow up.

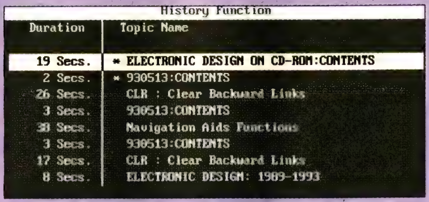
Glossary - Full article glossaries, provided by the Editors of Electronic Design magazine. The CD also comes with **WORD LINK**, which allows you to click on any word within the article and if it's in the glossary, the definition pops up. When you're done, a simple click and it's gone.

Navigation Aids - Magellan you're not, and you don't need to be!

All the aids you'll need to motor your way through this CD in no time flat.

CLR - *Clear Back Links* - Because every article you move to loads into RAM, this function allows you to clear articles you've finished. This frees up RAM for you to continue.

TOC - *Table of Contents* - Takes you directly to the Volume Table of Contents (the whole year) with special links provided to Issue T.O.C.


History Function

```
  Duration   Topic Name

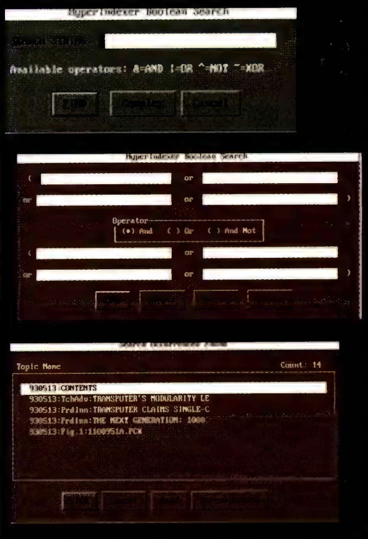
  19 Secs.   * ELECTRONIC DESIGN ON CD-ROM:CONTENTS
   2 Secs.   * 930513:CONTENTS
  26 Secs.     CLR : Clear Backward Links
   3 Secs.     930513:CONTENTS
  38 Secs.     Navigation Aids Functions
   3 Secs.     930513:CONTENTS
  17 Secs.     CLR : Clear Backward Links
   8 Secs.     ELECTRONIC DESIGN: 1989-1993
```

REL - *Show-Related Articles* - Calls up a list of, and lets you move to, related topics.

HST - *Show-Related History* - Shows each topic visited during your current session and how long you were there, and then lets you return to previous topics.

SEARCH dialog boxes

Simple search (top), Complex Search (center), and Search occurances found (bottom).


HyperIndexer Boolean Search

```
Available operators: &=AND |=OR ^=NOT ~=XOR
```

```
Operator
 (•) And   ( ) Or   ( ) And Not
```

```
Topic Name                                   Count: 14

 930513:CONTENTS
 930513:TchAdv:TRANSPUTER'S MODULARITY LE
 930513:PrdInn:TRANSPUTER CLAIMS SINGLE-C
 930513:PrdInn:THE NEXT GENERATION: 1000
 930513:Fig.1:1100951A.PCX
```

SRH - *Search* - Conduct simple, complex or proximity indexed searches.

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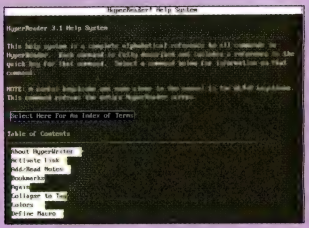
HyperReader! Help System

```
HyperReader 3.1 Help System

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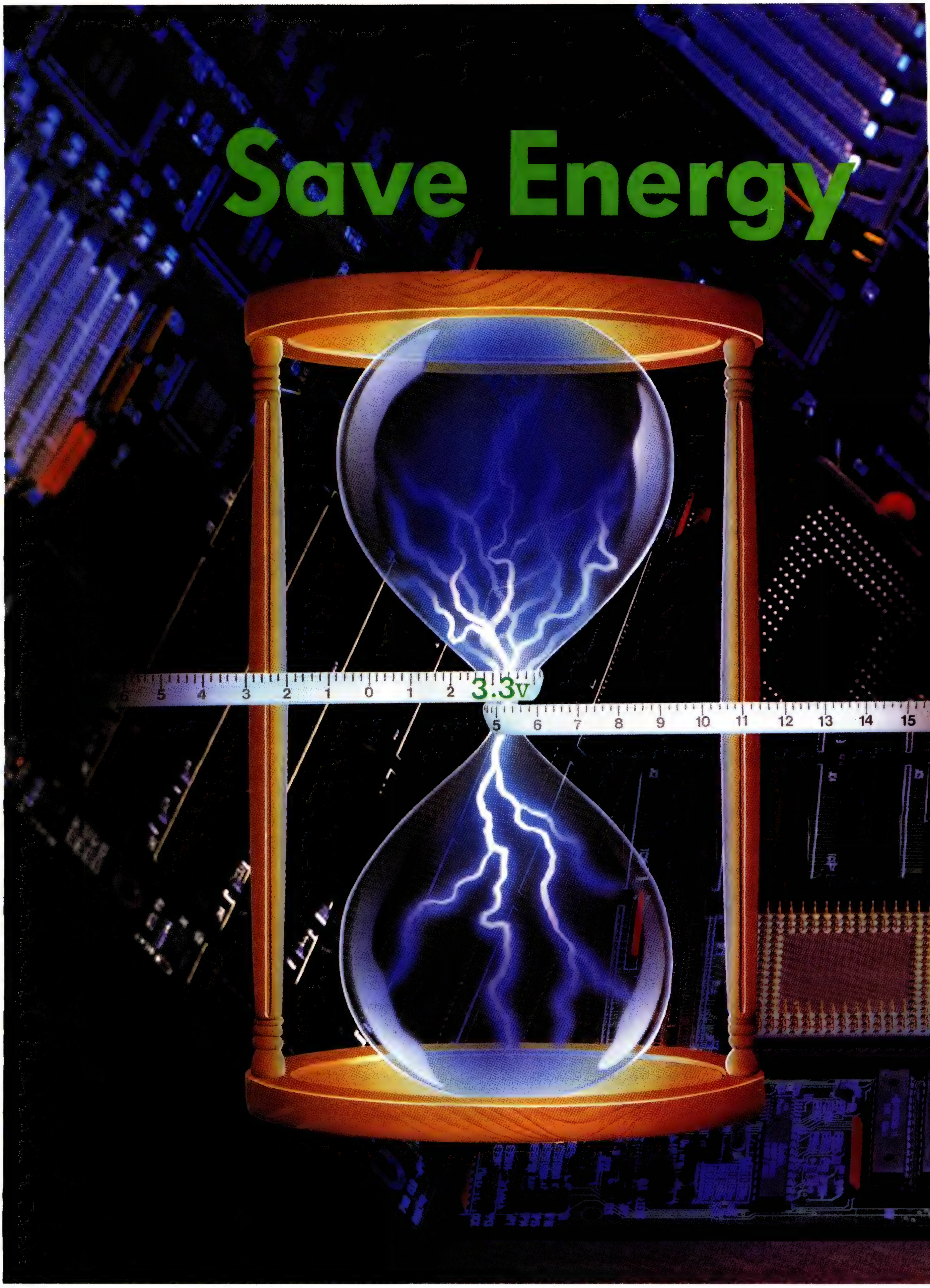

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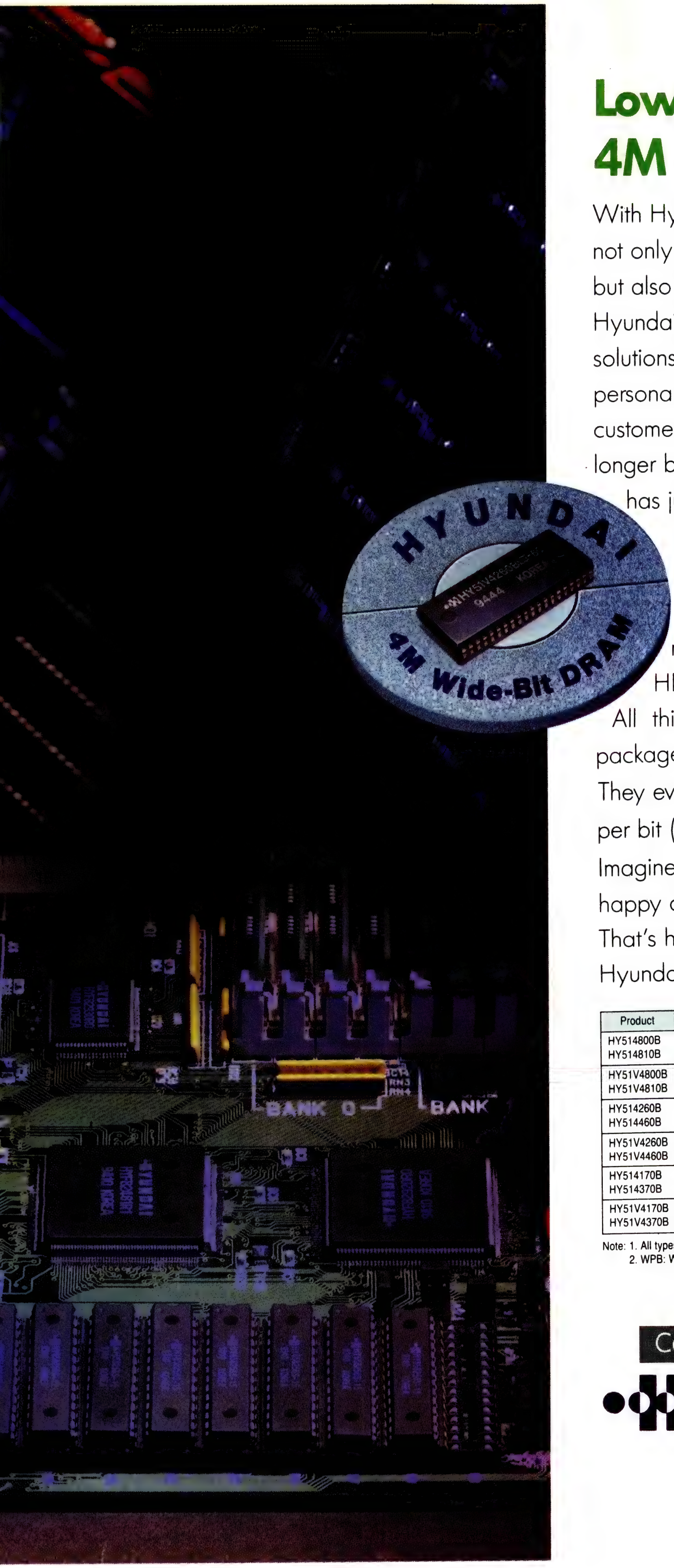

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HY514260B HY514460B	256K x 16, 2/CAS 256K x 16, 2/CAS WPB	L/P, S/R 512 Ref.	40 SOJ 40/44 TSOP-II	
HY51V4260B HY51V4460B	256K x 16, 3.3V 2/CAS 256K x 16, 3.3V 2/CAS WPB			
HY514170B HY514370B	256K x 16, 2/WE 256K x 16, 2/WE WPB	L/P, S/R 1K Ref.	40 SOJ 40/44 TSOP-II	
HY51V4170B HY51V4370B	256K x 16, 3.3V 2/WE 256K x 16, 3.3V 2/WE WPB			

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2. WPB: Write per Bit, L/P: Low Power, S/R: Self Refresh

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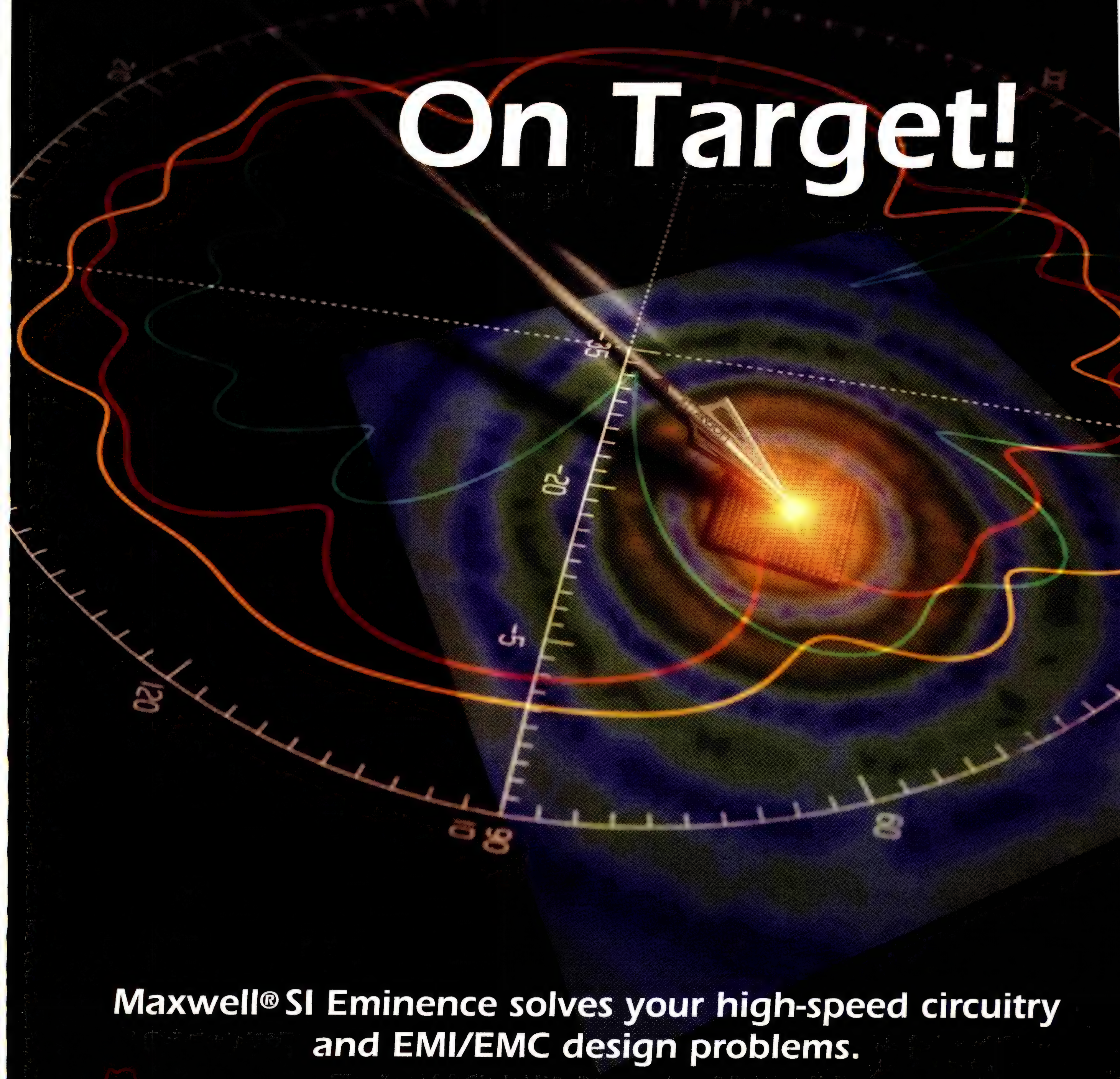

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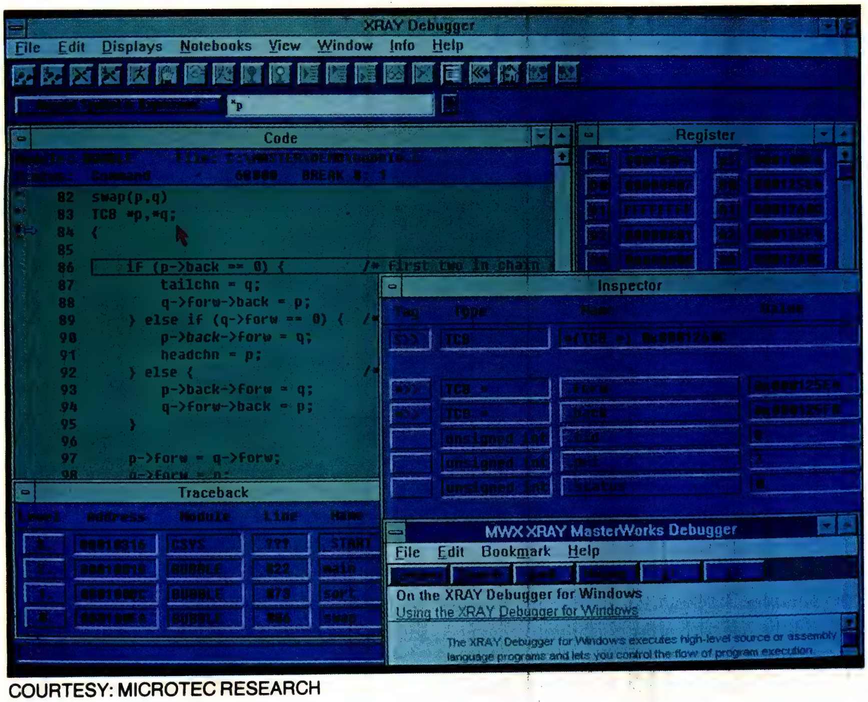


```
swap(p,q)
TCB *p,*q;
{

    if (p->back == 0) {          /* First two in chain
        tailchn = q;
        q->forw->back = p;
    } else if (q->forw == 0) {  /*
        p->back->forw = q;
        headchn = p;
    } else {                    /*
        p->back->forw = q;
        q->forw->back = p;
    }

    p->forw = q->forw;
```

On the XRAY Debugger for Windows

Using the XRAY Debugger for Windows

The XRAY Debugger for Windows executes high-level source or assembly language programs and lets you control the flow of program execution.

COURTESY: MICROTEC RESEARCH

ENGINEERING SOFTWARE TOOLS MEET DEMANDS

SHERRIE VAN TYLE

DESIGN TOOLS BECOME MORE FLEXIBLE AS INTEGRATED DEVELOPMENT ENVIRONMENTS GET SOFTWARE UP AND RUNNING FAST

The computer-aided systems engineering (CASE) umbrella covers system integration as well as software design and analysis methodologies. For the readers of *Electronic Design*, the most relevant concern is the point where hardware and software meet. Just as submicron design rules pack more functions on a chip than ever before, software engineering must meet the challenge of 32- and 64-bit embedded processors that manage sophisticated aerospace, telecommunication, and networking applications.

At the other end of the performance spectrum, millions of 8-bit microcontrollers are put to use each year to pilot subsystems in automobiles, appliances, and other equipment. Designers working with these systems must cope with task-timing problems and tight memory constraints. What's more, a new generation of distributed applications poses a fresh set of design, interface, and testing problems. Whether they're designing an 8- or 32-bit system, engineers working with embedded targets also are feeling the pinch of shorter time-to-market. That often means writing and debugging the application concurrently with hardware development.

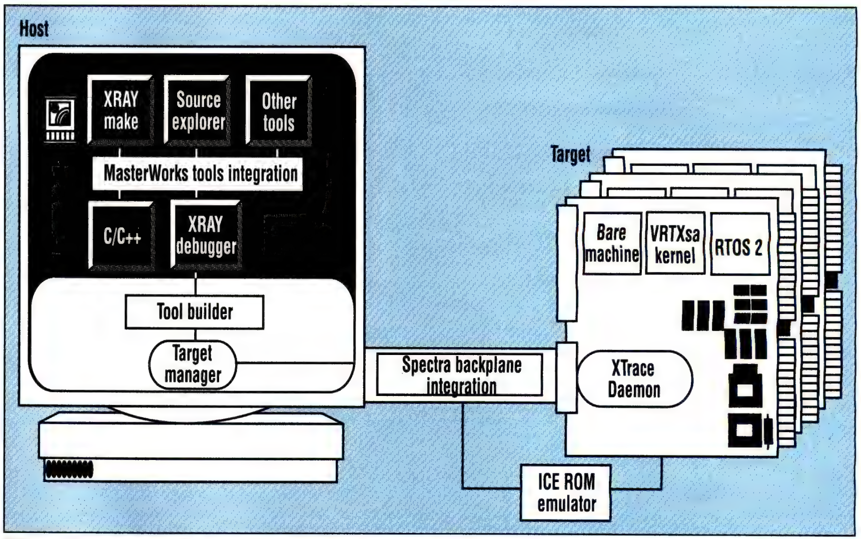
Yet debugging real-time and embedded applications can be difficult and time-consuming because the programs that run instruments, laser printers, telecom switches, and other equipment typically are multithreaded. That is, various tasks are assigned priorities and scheduled to execute on the microcontroller. Although the tasks and interrupt service routines (ISRs) in an application program may run without a hitch individually, together they can cause missed timing deadlines, race conditions, and deadlocks. When a processor crashes, a likely culprit is a snag in the scheduling of the many tasks running—even an 8-bit design can have 60 or so tasks assigned.

Fortunately for designers, a new generation of tools is arriving to help developers sort out these timing issues and fix other real-time problems. At a nuts-and-bolts level, optimizing compilers for C programs have made developing in C feasible for applications with tight memory constraints. On development and debugging platforms, graphical user interfaces as well as actual Windows implementations running on PCs are supplanting traditional command-line entry of debugging directives. Multiple windows on-screen helps embedded-system designers monitor how tasks interplay as well as troubleshoot programs interactively. The most sophisticated tools feature integrated development environments, which can minimize the time designers spend getting tools to work smoothly together. These environments make up a complete operating system, which typically consists of a real-time kernel, compiler, debugger, language-interface libraries, network manager, and file-management executive.

Still, designers at smaller companies are reluctant to invest thousands of dollars for a tool environment, which would include royalties for each system sold. For systems built around 8- and 16-bit microcontrollers, designers most often will write their own operating system and application and rely on off-the-shelf compilers, debuggers, and linkers; hardware emulators; and logic analyzers to polish code.

Obviously, vendors of real-time operating systems and development environments have a stake in bringing developers into the fold. A driving force is time-to-market pressure; the time to write a kernel includes debugging, documenting, and maintaining the code. Code written in assembly for one processor isn't portable to any other processor. What's more, code written under tight deadlines probably isn't documented and, as a result, isn't reusable. For large applications, designers may first turn to software-analysis tools *(see "Software analysis: Finding a methodology," p. 74)*.

Choosing an environment isn't easy, though: At one count, there were at least 40 companies marketing real-time kernels and operating systems, with some supporting one chip or one family and others targeting a broader range of processers; for example, JMI Software's C Executive, which is written in C with small amounts of processor-specific code, runs on at least 20 different processors.



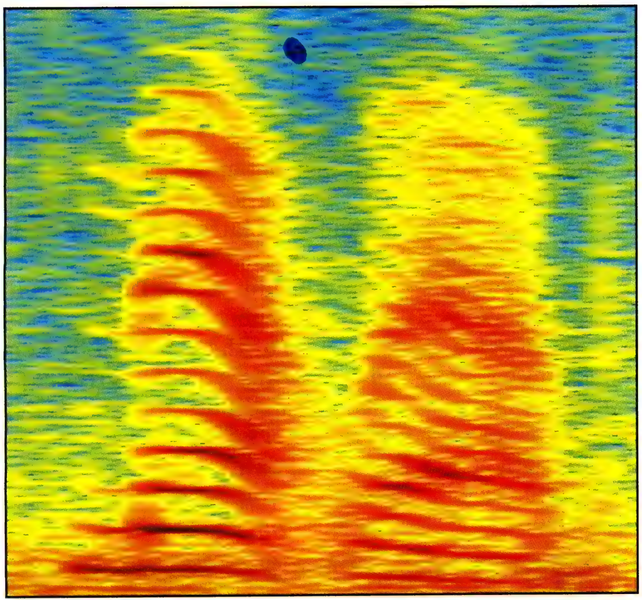
1. AS PART OF THE OPEN DEVELOPMENT ENVIRONMENT of Microtec Research, XRAY MasterWorks and the Spectra cross-development backplane work side by side with other compilers, debuggers, and real-time OSs.

For designers debating whether to buy tools or "roll their own" kernel, books and conferences on embedded-system design can be useful. For example, in the book, *μC/OS: The Real-Time Kernel*, author Jean J. Labrosse describes the workings of his own portable, ROMable, preemptive multitasking kernel. Because Labrosse supplies C source code, readers can tailor the kernel to their system by adding features (he recommends that readers be familiar with ANSI C and assembly language for Intel's 80x86 family).

For designers pressed to get an application running as quickly as possible, integrated tool environments make sense. Tool makers report that embedded-software developers want tools that supply seamless links between editing, compiling, and debugging. Still, matching the requirements of an application to a tool environment is a challenge; designers need to gather information about kernels from vendors on such issues as interrupt latency and system performance in relation to the number of tasks. Also, for designers attached to a particular compiler or debugger, it makes sense to find out if the environment can work with these tools. For example, an increasing number of popular compilers work with integrated environments.

At least one supplier of development environments recognizes that many designers are working with low-cost, high-volume, compact applications with only 3 to 6 kbytes of ROM. Microtec Research Inc., Santa Clara, Calif., introduced the VRTXmc real-time kernel with one-third the RAM size of the VRTX32 kernel. A subset of the VRTXsa kernel, it adds a virtual timer function and stack-memory usage measurements to the VRTXsa's standard features of mailboxes, event flags, and priority-based preemptive scheduling. The ability to examine a processor's stack overflow/underflow condition is key in compact applications. Designers working with the VRTXmc kernel can use Microtec's Spectra cross-development backplane or the XRAY Debugger in standalone form. The XRAY MasterWorks development environment enables developers to incorporate other compilers, debuggers, and even other real-time OSs *(Fig. 1)*.

The pressure to develop a product quickly is especially strong in consumer devices like personal digital assistants (PDAs), interactive video systems, and set-top devices. Other active areas include networking tasks, such as wired and wireless local-area-network (LAN) controllers, hub controllers, and PCMCIA modem cards. As an example, the ARM 32-bit RISC processor developed by VLSI Technology, San Jose, Calif., is



MATLAB simplifies analysis and algorithm development with integrated modeling, design and graphical tools. This spectrogram shows how a speech signal varies with time and frequency.

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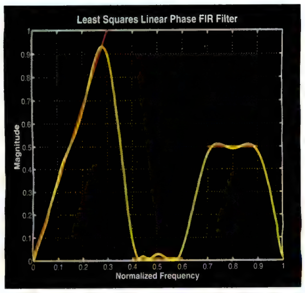
The MATLAB Signal Processing Toolbox is a powerful interactive environment for signal analysis, algorithm development, and DSP design.



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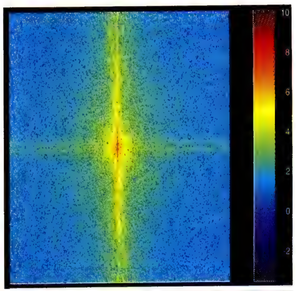

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implemented in the Apple Newton and other consumer devices. To allow for quick writing and debugging of code, the company created JumpStart development tools that let developers write C and assembly-language code for the ARM processors in an integrated environment.

Tom Schild, product marketing manger for embedded products at VLSI, says that being able to debug code faster is important for designers who have to cope with shortened design cycles to meet market introduction times. The JumpStart environment includes tools to compile, link, debug, and optimize application software. When a developer needs to look up information in the documentation, he can click on on-line help to access hypertext-linked specifications and instructions.

A graphical makefile utility helps manage and track products by constructing and executing user-defined files and commands. Developers can browse and edit source code with the toolset's dynamically linked windows. JumpStart also has an interactive C-code debugger with conditional stepping, dedicated backtrace, and performance windows for debugging and further code optimization. The tool includes a portable run-time ANSI C library and an ARM instruction-set emulator for target simulation. The tools run on Sun and HP platforms, with a Windows version in the works.

Though built around a different processor, shorter time-to-market also is part of the appeal of System and Software's (SSI) SoftProbe 386EX/SIM Simulator/Debugger tool for Intel's 80386 EX processor. The Irvine, Calif., company's simulator enables engineers to develop applications for the processor before

SOFTWARE ANALYSIS: FINDING A METHODOLOGY

The reason for all the interest in software-engineering methodologies is that we all recognize that software development is very complicated and that existing methods are extremely labor intensive and error prone. Writing software is "details" work. It is very common that we can't see the forest for the trees when we write software. As systems continue to get bigger and more complicated, theoreticians try to help us by providing techniques for organizing our thoughts and our software to make our systems more robust and easier to change.
Excerpted from Karen S. Ellison's book *Developing Real-Time Embedded Software In A Market-Driven Company.*

With increasing demands for higher quality and reusability, developers upgrading, documenting, testing, and reengineering large software programs now have an array of tools to choose from. One difficulty is matching the right CASE tool and methodology to the problem domain. At last count, at least a dozen approaches to modeling are implemented, some more applicable to developing real-time software than others.

Originating at Bell-Northern Research and now developed by ObjectTime, Kanata, Ontario, Canada, the toolset of the same name is aimed at real-time systems, including complex, distributed applications such as telecommunications network modeling, protocol design, system architecture, and software design using C++. Rather than adapt software-design methodologies from other problem domains, ObjectTime supports the Real-Time Object-Oriented Modeling (ROOM) methodology. Its object-oriented capabilities are intended to create reusable large-scale design components, not just reusable code.

According to Paul Ward, codeveloper of the Ward-Mellor real-time development approach, ROOM overcomes the limitations of early real-time structured techniques by adding sophisticated state-machine support and object orientation. It is superior to general-purpose object-oriented methods in that it was conceived and optimized exclusively for real-time development.

Object Time/ROOM enables developers to specify networks of interacting concurrent processes (Actors) for either abstract or detailed design. Protocols can be defined through strongly typed interfaces. It supports inheritance and has graphical architecture/design capture. The methodology allows multiple design views as well as generic Actor-class substitution.

For programming, the tool permits batch-mode design compilation. It has a Rapid Prototyping Language, and supports C++ standard libraries. It can be imported or source-developed externally. With executable models tied into prototype user interfaces, developers can engage customers early in product development to verify features of the system under development. Real-time domain concepts include networks of interacting concurrent processes, hierarchical finite-state machines, formal protocol definitions, and support for layering. It supports basic or discrete-event simulation models (to model processing delays or message transfer delays).

One characteristic that distinguishes the *001* CASE tool suite developed by Hamilton Technologies, Cambridge, Mass., is that it was self-generated from the development before-the-fact paradigm, creating reliability and integration within the toolset. The suite's hierarchical mapping tools, FMaps and TMaps, capture data flows, data dependencies, timing, priority, ordering, parallelism, as well as the structure and characteristics of all objects in the system. The suite's Analyzer tool tracks errors in the hierarchies and the resulting network of intercommunication functions. The Resource Allocation Tool can be programmed to add new sets of language primitives. The toolset also contains an Xecutor, which target hardware is available. Tom McCloud, Intel Corp.'s marketing manager for embedded-processor operation, points out that developers using the simulator can have their applications ready at the same time that 386EX silicon will be delivered.

The DOS-based SoftProbe tools enable engineers to simulate the processor's functions at the bus and instruction level. Engineers also can debug, via software simulation, their real- and protected-mode C/C++ and PL/M applications for the 386X. The tools enable debugging of code, such as real/protected-mode switches, that in-circuit emulators can't track. One advantage of working with the 386 architecture is that many hardware and software engineers work on PCs and are familiar with the processor's architecture and the tools that work with it. The simulator is compatible with popular compilers, linkers, and assemblers, including MetaWare's High C/C++ Optimizing Compiler, Watcom/386 32-bit Optimizing Compiler, Microsoft C/C++ Optimizing Compiler, System & Software's Link & Locate 386, and Microsoft's MASM Assembler.

The simulator aims to form a "bridge between bare bones and C." SSI's vice president of technology development, Wilson Chan, wrote a guide that takes a developer through writing a 386-protected-mode flat model-C program, an embedded application using a 32-bit C compiler, a macro assembler, and an embedded linker. The guide, *Writing ROMable Code For The 386*, discusses using C for embedded systems. It covers issues like run-time library support and floating-point math support, including a math coprocessor and an emulation library. One chapter goes through step-by-step instructions for building an example embedded 32-bit C++ program, which is compiled using a small-memory model.

The embedded program is built using the protected-mode, flat-model assumption. The chapter on run-time libraries covers the MetaWare High C/C++ compiler. Included in the compiler is a run-time library (small memory model only) that supports a DOS environment. As the name suggests, DOS-independent functions require no support from DOS and can be used directly in embedded applications. Functions marked "reentrant" may be employed simultaneously by more than one independent program or task. Functions marked "intrinsic" aren't available in the run-time library; the compiler generates in-line code for them directly, saving the overhead of a function call.

Microtek International's PowerPack-386EX in-circuit emulator can help developers working with Intel's embedded 386 chip. Its PowerViews interface, which runs under Windows 3.1, incorporates such Intel-specific features as memory addressing, I/O triggering, a system-management mode, and a disassembler. Debugging features include a variable window, a stack browser, multiple memory windows, and a deep trace with a linked cursor-to-source window. The Hillsboro, Ore., company's emulator supports compilers from Borland, Metaware, Microsoft, MRI, and Watcom.

CE-Macro 386 developed by JMI Software Systems, Spring House, Pa., supplies a set of Soft-Scope III macro commands for debugging

can simulate a system. The OMap Editor provides a visual means of examining objects and debugging generated code at the back end of the process.

Cadre Technologies Inc. has enhanced its Teamwork automated development tool. Besides an improved user interface, Release 6.0 of the toolset includes ShortCut for rapid prototyping; Dynamic Analysis for dynamic model verification and debugging; enhanced reverse engineering and metrics for Ada; and improved documentation generation. The Providence, R.I., company has also enhanced the ObjectTeam object-oriented development tools, which automate the Shlaer-Mellor and Rumbaugh *et al* methods. Recursive design support has been added to ObjectTeam for Shlaer-Mellor, which enables the generation of executable code from an analysis model of an application. Also included is a template for generating C++ code.

Although object-oriented design and analysis of software (OOA/OOD) is growing in popularity, much existing software was designed with structured programming techniques. Along these lines, Interactive Development Environments (IDE), San Francisco, overhauled its original tool for structured analysis and design. The rebuilt StP/SE supports design diagrams and notations for most popular structured methodologies, including Yourdon/DeMarco, Gane/Sarson structured systems analysis, Hatley/Pirbhai real-time extensions, Jackson hierarchical data structures, Yourdon/Constantine design, and the Watts/Humphrey software process model. The toolset builds on "Software Through Pictures" core technology, including a shared repository that stores analysis and design information in one central location. Because the upgrade is better integrated with other software tools, designers can use such integration frameworks as Hewlett-Packard's Soft Bench. The tools also support document-generation tools like FrameMaker or Interleaf. Configuration management duties are automated.

For individual developers working seeking more powerful browsing and lint-type error checking for working with large programs, Procase Corp., San Jose, Calif., has come up with a single-user version of Smartsystem. With the software's error analysis and browsing features, developers can pinpoint errors in the source code, view dependencies, make changes, and quickly see the effect on the rest of the program. Because Smartsystem works on code that doesn't compile successfully and on code targeted for other platforms, upfront error analysis saves time in producing quality code.

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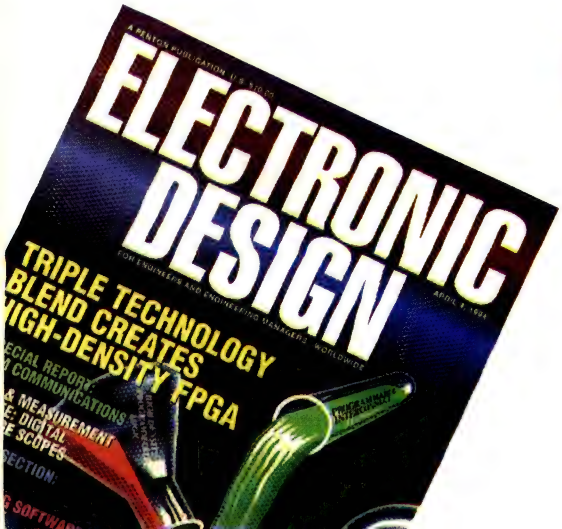

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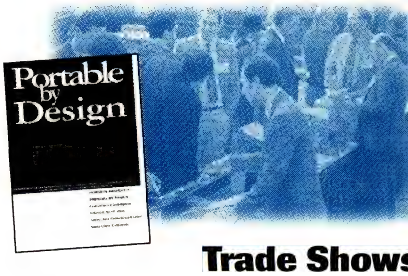

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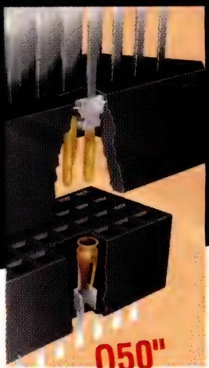

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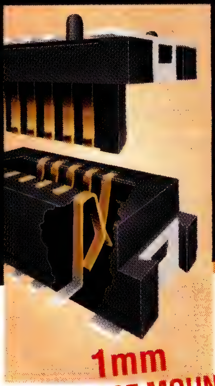

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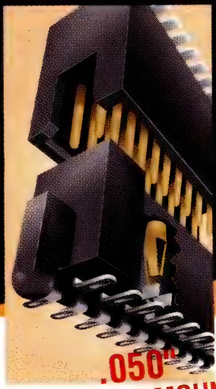

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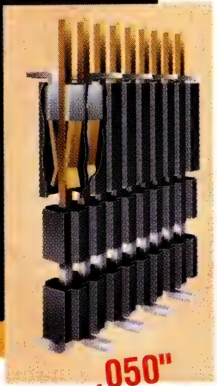

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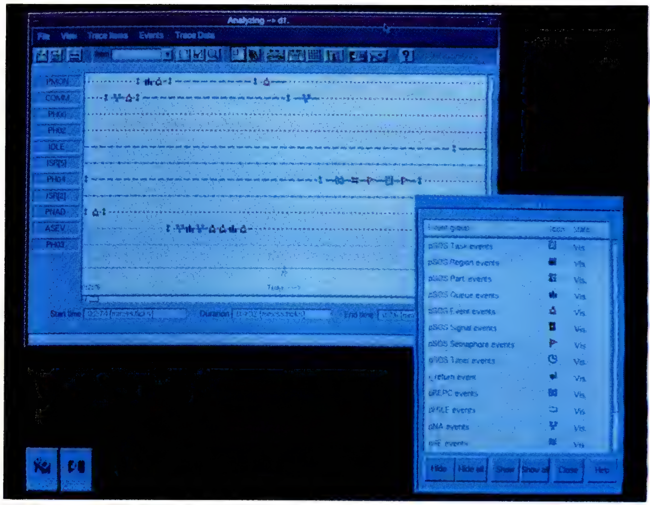
386/486 systems based on the C Executive real-time kernel. Soft-Scope III, a debugger from Concurrent Sciences, supplies remote debugging of embedded 386/486 software written in C or assembler. The macro commands extend Soft-Scope to display information about task status and kernel configuration.

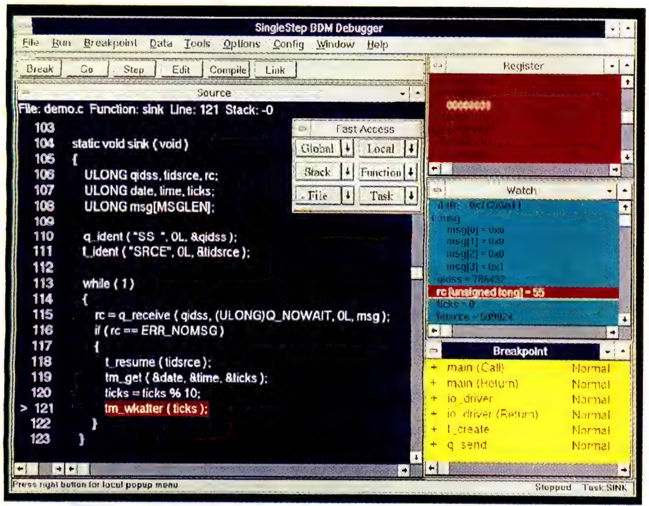
PORTING TOOLKIT

To leverage the popularity of Motorola's 68040 processors, Microware Systems Corp., Des Moines, Iowa, offers a developer's license kit for porting applications built on its OS-9 operating system to new 68060-based platforms. Developers can use the kit to build a ROM-based or flash-memory-based embedded controller, or a networked multiprocessor system. It combines object code with version 3.0 of the operating system, as well as source code for the operating system's core file managers. Because of its I/O file-management capabilities, it's especially suited for interactive video and other multimedia applications. Supported are ISDN, Ethernet, MPEG, SCI, real-time audio/video, and industrial digital/analog I/O applications. The kit has installation source code for boot code and device drivers, and can be installed on up to five in-house targets.

Also aimed at 68000-based applications, SingleStep++ is the first software development environment for embedded applications licensed by Microsoft to run under Windows. Created by Software Development Systems, Oak Brook, Ill., the environment offers a background debugging mode (BDM), which is rare for real-time debuggers *(Fig. 2)*. As a result, developers can monitor real-time applications that run continuously. Developers can perform target diagnostics right from the PC, enabling them to correct stack overflows that often occur in real-time applications. Single Step++ provides fast instruction-set simulation, executing 5000 instructions/s.



3. GIVING A VIEW of an application's multitasking operations, ESp software from Integrated Systems helps designers examine memory use and demands on CPU resources. The analyzer window maps executions of tasks, interrupts, and objects over time, using icons to show events like context switches, interrupts, and semaphores. Users can filter unwanted tasks and group tasks to be examined.



File: demo.c Function: sink Line: 121 Stack: -0

```
static void sink ( void )
{
   ULONG qidss, tidsrce, rc;
   ULONG date, time, ticks;
   ULONG msg[MSGLEN];

   q_ident ( "SS  ", 0L, &qidss );
   t_ident ( "SRCE", 0L, &tidsrce );

   while ( 1 )
   {
     rc = q_receive ( qidss, (ULONG)Q_NOWAIT, 0L, msg );
     if ( rc == ERR_NOMSG )
     {
       t_resume ( tidsrce );
       tm_get ( &date, &time, &ticks );
       ticks = ticks % 10;
       tm_wkafter ( ticks );
     }
  }
```

msg[0] = 0x0
msg[1] = 0x0
msg[2] = 0x0
msg[3] = 0x1
qidss = 786432
rc [unsigned long] = 55
ticks = 0

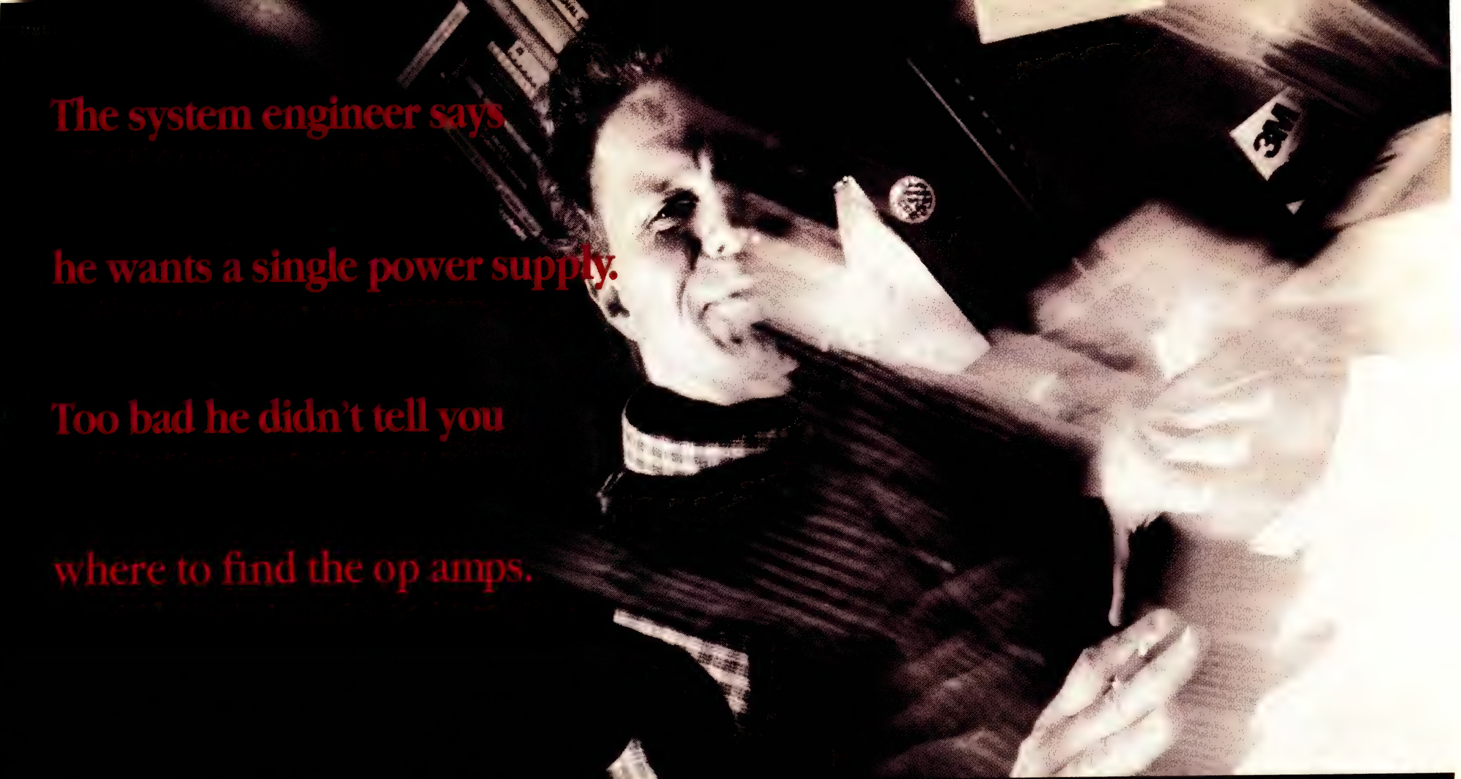
+	main (Call)	Normal
+	main (Return)	Normal
+	io_driver	Normal
+	io_driver (Return)	Normal
+	t_create	Normal
+	q_send	Normal

2. BY INTEGRATING program building, code generation, debugging, and analysis tools, SingleStep++ can support background-mode debugging with Motorola's 68300 processors. It's the first Microsoft Windows-licensed embedded development environment.

In keeping with trends of OS portability and scalability, an example of a scalable microkernel is the OS from Chorus Systems, Beaverton, Ore., the U.S. arm of Chorus Systemes, SA of Cedex, France. Because Chorus/MiX's microkernel-based operating system is machine-independent, modular, and scalable, it's suitable for distributed applications. To assist developers, the Chorus/MiX evaluation program includes training, consulting, and support as well as hands-on experience with the Chorus/MiX microkernel-based operating system. With its binary evaluation package, developers can use Chorus in a preliminary design. A source-evaluation package gives access to the Chorus/MiX source code with support from Chorus Systems in detailed design and prototyping.

Another trend is the integration of tools and kernels from different vendors. One example is the compact, ROMable RTXC real-time OS designed by Embedded System Products, Houston, Texas. It's integrated with Software Development Systems' SingleStep++ and CrossCode++ development and debugging environment. Similarly, Integrated Systems Inc.'s (Santa Clara, Calif.) pSOS+ and pSOSm kernels are integrated with SingleStep++. In this configuration, engineers develop applications on a PC-compatible host computer running Microsoft Windows, connected to a target system running either pSOS or pSOS+m embedded real-time kernels. At the high-performance end of embedded systems, Digital Equipment Corp., Maynard, Mass., is integrating unified OSF/1 Unix with real-time extensions and VxWorks for its Alpha 64-bit RISC AXP processors. C Executive from JMI Software Systems now runs on the MIPS R4000 processor, using the Green Hills C compiler.

For its pSOS+ and pSOS+m real-time applications, Integrated Systems created the ESp Intuitive Visual Debugging tool *(Fig. 3)*. The analyzer window maps execution of tasks, interrupts, and objects over time. Events are marked with such icons as context switches, interrupts, and semaphores. Filtering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OP	113	213	413		•	•	•			75	4.7	±40	1.75	3.4	Lowest noise and drift
OP	183	283		•	•	•	•			1000	10	±25	1.5	5	5 MHz from +3 to +36V
OP	90	290	490	1.6	•	•	•			150	60	+13/-7	0.015	0.02	Precision micro power
OP		291	491		•	•		•	•	700	21	±10	0.35	3	Low power R-R I/O
OP		292	492		•	•	•			800	15	±8	1.4	4.5	Low cost
OP		295	495	•	•	•	•		•	300	45	±18	0.15	0.075	Accuracy and output drive
AD	820	822		•	•	•	•		•	400	16	±30	0.8	1.9	FET Input
SSM		2135			•	•	•			1000	4.7	±40	1.75	3.5	Excellent for audio
AMP04					•	•	•			150	25	±15	0.7	0.3	Easy-to-use +5V inst. amp
AD626				•	•	•		>		250	250	15	0.23	0.1	Low cost diff. amp

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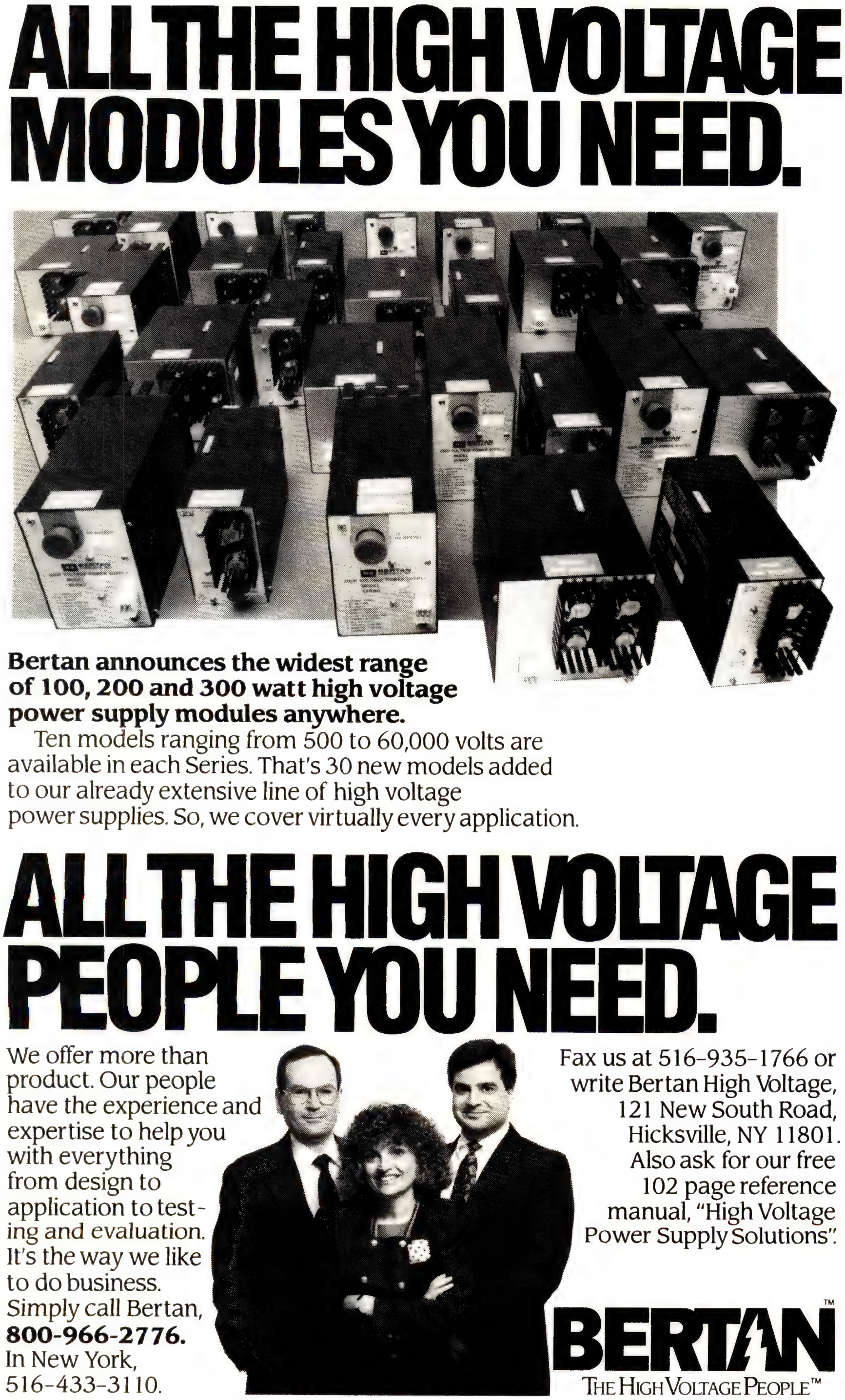

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and grouping features let users view only the tasks and objects critical to the application, which is useful when sifting through dozens of tasks in a multithreaded application. Sampling rates can be set to 1-μs resolution.

MONITOR STACKS

As noted earlier, because effective memory management looms large in developing embedded applications, ESp's run-time profiling meters enable users to monitor stack usage on running applications. CPU performance meters display computational intensity of running applications and signal potential performance bottlenecks. Other meters show frequency of I/O calls, interrupts, service calls, context switches, and user events.

Engineers can configure the size of the data-collection buffer, filter the data collected, insert user-defined events, and select from data-collection triggers. Data can be collected in time-based, event-based, or wraparound modes, which allows the application to run until failure. This feature particularly beneficial in diagnostics.

Looking to the future, among the companies offering development environments to support the PowerPC embedded processors are Microware and Microtec Research, which plans to release support for the processor with its XRAY MasterWorks C/C++ development environment.☐

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COMPETITIVE VIDEO COMPRESSION-DECOMPRESSION SCHEMES FORGE AHEAD

Though Motion Video On PCs Is Still In Its Infancy, Designers Now Can Get A Good Feel For Which Technology Best Suits Their Needs.

BY RICHARD NASS

As video-on-the-desktop forges closer to reality, multimedia developers continue to explore the different methods of video-data compression and decompression. Presently, several video compression/decompression techniques are vying for the spotlight. The best technique, however, depends on the particular application.

Personal-computer designers envisioned video on the PC many years ago. The original Multimedia PC (MPC) council, anticipating the video trend, set forth a standard MPC platform that has since been upgraded. This standard platform is necessary for each and every technique employed.

The minimum configuration for an MPC-compliant platform consists of a 25-MHz 486SX microprocessor; 4 Mbytes of DRAM; and a double-speed CD-ROM drive with a 300-kbyte/s sustained transfer rate, 40-ms average seek time, and a 64-kbyte onboard buffer. Also included are a VGA-resolution (640 by 480 pixels) display that can handle 65,000 colors; MIDI (musical instruments digital interface) and joystick I/O ports; and an audio board.

One standard that seems to be garnering much popularity is the Motion Pictures Experts Group (MPEG) scheme. However, there are other techniques that should not be discounted, such as Captain Crunch, Indeo, and Cinepak (each of which are discussed later in this article).

The MPEG algorithm is built around a discrete-cosine transform (DCT) algorithm. The DCT method breaks the video signal up into blocks of 8 by 8 pixels. Those blocks are then transferred from the spatial domain to the frequency domain by implementing a cosine transform, which is similar to one-half of a Fourier transform. In the frequency domain, elements that aren't visible with the human eye because they're masked can be removed. Once the blocks are transformed, motion estimation is performed on the video signals, where the system tries to determine whether a block has moved or actually changed. Because the *DCT* technique is extremely computationally intensive, expensive hardware is typically required to handle the MPEG encoding.

MPEG, a subset of the video-CD standard, is basically a data-interchange standard. The video-CD specification defines the way that data is recorded on the disk, in what format, where the header is placed, what kind of directory is employed, and so on. It also handles the aspects of the MPEG scheme that aren't compression-related, such as fast-forwarding and reversing.

ORIGINALLY FOR CDS

The original MPEG-1 standard was developed for compact discs (CDs). It works by recognizing that pixels change little from frame to frame in moving video images. The system takes a reference frame, compresses it, performs a transform, then quantizes the frame. This four-step procedure retains all of the information, thus maintaining high quality. Then the system takes a new refer-

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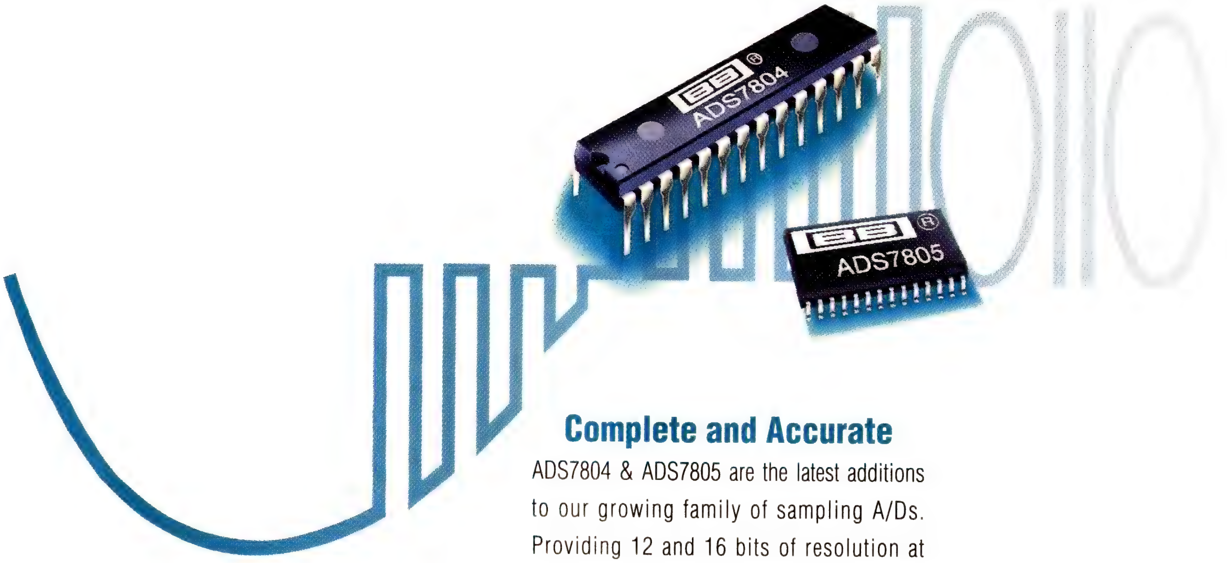

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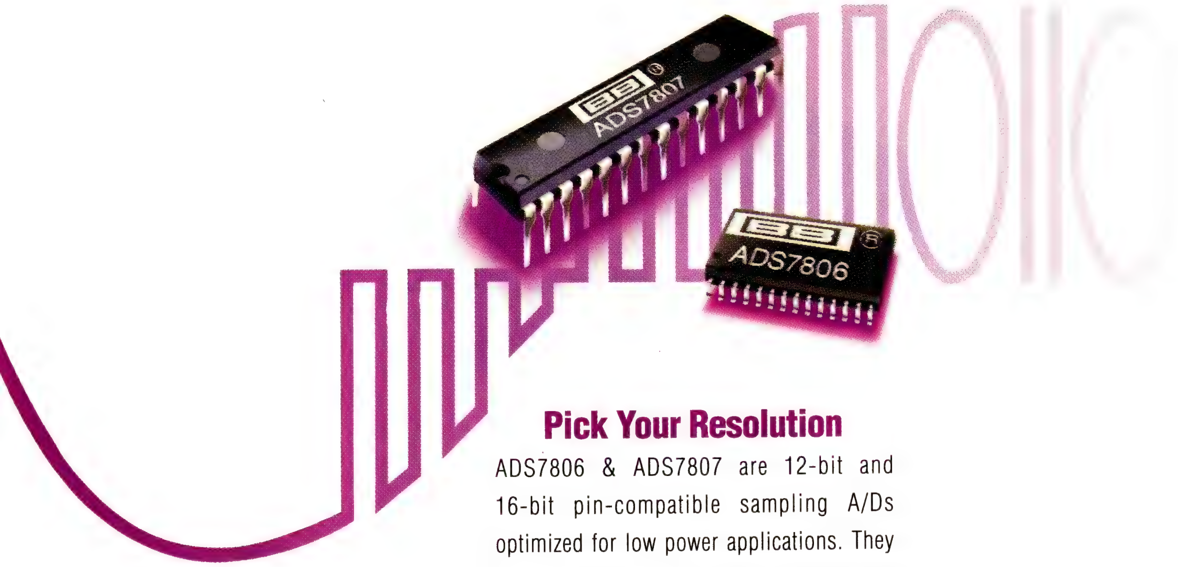

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ence frame, about three or four times per second, depending on how much pixel movement occurs. In between reference frames, the system transmits vectors to signify which areas in the frame have moved, and in what direction. Between the motion vectors, predictions are made to determine where the next movements will occur.

The MPEG-1 specification calls for a maximum compressed bit-stream data rate of 1.5 Mbits/s. But after the specification's inception, the committee removed that upper bit limit.

MPEG-2 came into play when higher resolution applications became popular, such as digital television. In addition to the higher resolution, the specification also has the hooks built in for interlaced or noninterlaced displays. MPEG-2 actually has a number of profiles and levels, with different bit rates for each level and profile. Typically, designers refer to the main level and profile, which has a bit rate of 15 Mbits/s.

Many MPEG-2 developers have been slow to complete their designs because, until recently, the specification has been a moving target. With the standards body essentially completing the draft for MPEG-2, developers can move to the next design phase feeling more confident that the specification will remain intact.

SUPPORT PRODUCTS

Video-CD support chips and board-level products have started to find their way into the marketplace *(see "Low-cost video CD chip set," below)*. C-Cube Microsystems, Milpitas, Calif., recently developed a RISC-based chip that decodes MPEG and other video-compression algorithms. With multimode video capabilities, it eliminates interoperabi-

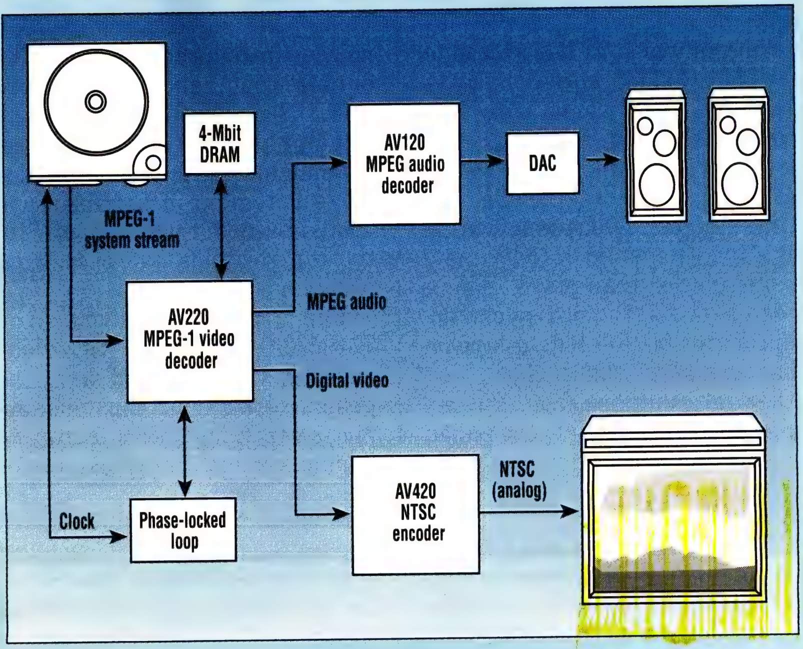
LOW-COST VIDEO CD CHIP SET

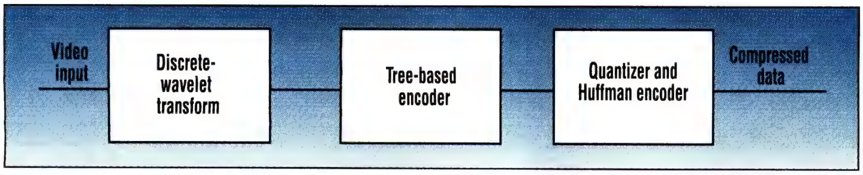
While business audio and video is a hot topic among PC developers, there's a related market that's poised to emerge—video CDs. Video CDs, which fit the same form factor as audio CDs, will be used for karaoke, movies, music-video playback, interactive video games, and educational programs. To accommodate that market, Texas Instruments Inc., Dallas, developed a chip set that supplies the logic needed to build a full-motion video subsystem.

The video CD standard was developed by JVC, Matsushita, Philips, and Sony with the intent to expand the capability of the CD as we know it today. The standard is backward-compatible with the current audio CD format. This means that full-motion video can be stored and combined with high-quality audio. The standard defines the data format on the disk so that any compliant player can read it. Then the player relies on an MPEG-1 audio and video decompression system to handle the playback.

TI sees the largest initial market for these playback systems in Asia and Japan in home karaoke systems. The company claims that there are already over 900 titles available in the video CD format. "I think a lot of people have ignored this MPEG-1-based video-CD equipment that's coming out," says Ron Slaymaker, manager of TI's Digital Compression Products group. "We think the video CD will be the first high-volume use of the compression technologies." In addition, video CDs give movie-production houses a new distribution medium. The format has many advantages over VHS tape, such as its long-term reliability and higher-quality audio.

The chip set gives designers of these end-equipment applications a canned easy-to-use solution that's optimized for video CDs. System designers thus can get their products to market quickly while hitting the price points that are necessary for this type of application. Specifically, the chip set decodes, synchronizes, and decompresses the encoded audio and video data using the MPEG-1 scheme. Then it outputs a video signal encoded in the NTSC format. In addition, it outputs an audio signal that can be played back either over a standard TV or a high-fidelity stereo system to at-





1. The Captain Crunch compression algorithm, developed by Media Vision, passes data through three stages. These are the discrete-waveform transform, the tree-based encoder, and the quantizer and Huffman encoder.

lity issues for hardware developers seeking a wide range of video-compression support. The part also handles all main video standards, such as NTSC and PAL.

C-Cube's CL9100 16-bit CPU supports main-level, main-profile MPEG-2 video streams at rates up to 15 Mbits/s. It handles horizontal resolutions of 352, 480, 544, 704, and 720 pixels, and vertical resolutions of 240, 288, 480, and 576 pixels. A companion part, the CL9110, implements MPEG transport-layer demultiplexing. Also based on a RISC architecture, the CL9110 processes the transport and packetized elemental-stream layers of the data streams. It supports channel rates of up to 60 Mbits/s and connects to the CL9100 and an MPEG audio decoder without any glue logic.

Another MPEG-2 IC comes from LSI Logic Corp., Milpitas. The L64000 video decoder supports NTSC and PAL display formats and can perform all of the functions required for integration into a set-top decoder box. These features include support for channel switching, closed captioning, audio and video synchronization, and time-base correction. Because the decoder IC contains an on-chip display buffer and display-buffer controls, the only external circuitry required is a low-cost 8-bit microcontroller to handle initialization, status monitoring, testing, and near real-time device programming.

One of the first board-level MPEG playback solutions comes from Sigma Designs Inc., Fremont, Calif. The company's ReelMagic controller board handles 16-bit MPEG video and audio playback. The ReelMagic Lite board offers similar video capabilities, but requires a separate audio subsection. It can handle full-screen, full-motion video at 30 frames/s. The ReelMagic board sells for $449 and comes bundled with utilities and other MPEG titles. The Lite Board costs $100 less.

One of the deficiencies of the MPEG scheme is its need for a huge amount of processing power to perform data compression. However, on the positive side, decompression is fairly simple.

tain the benefits of high-quality audio.

The video-CD chip set consists of three devices: a video decoder, an audio decoder, and an NTSC encoder. A digital-to-analog converter, a 4-Mbit DRAM, a phase-locked loop, and the TI chip set are essentially all that's needed to add the video-CD capability to an existing audio CD player *(see the figure)*.

The video decoder, the TMS320AV220, was created as part of a relationship with C-Cube Microsystems. TI and C-Cube have a technology-exchange agreement concerning MPEG decoding, in which TI has access to any MPEG video work done by C-Cube, and vice versa with TI's work in the audio domain.

The AV220 employs the C-Cube MPEG Video 1 core (C-Cube calls it the CL-450), which is joined by an MPEG-1 system decoder. As a result, rather than just handling video packets, the device can accept a full MPEG-1 data stream that includes audio, video, and other information. Also, the microcode load and storage is pulled on-chip and has a direct interface to some of the popular CD-ROM decoders.

The video decoder also handles the audio and video synchronization in the MPEG system, taking the burden off system designers. The part also offers direct interfaces into the NTSC-encoder and audio chips, eliminating the glue logic that would be necessary if discrete devices were employed from multiple vendors. Finally, some of the video-control functions, such as fast forward and reverse, are included and supported as part of the video decoder.

The audio decoder, called the TMS320AV120, is a second-generation part. Even though it's less expensive than its predecessor, the AV110, most of the mathematical analysis that was done for the AV110 carried over to the AV220. This makes sure no quantization noise is introduced into the audio output when audio with more than 16 bits is employed. The part wasn't built with a standard programmable digital-signal processor—a dedicated architecture was designed that's specific to these algorithms and associated functions.

The final device, the TMS320AV420, an NTSC video encoder, was designed from the ground up for these consumer applications. It includes a feature to handle vertical interpolation for enhanced video quality. This feature is specific to MPEG-1-based applications. The part includes synchronized timing generation for the MPEG video decoder as well.

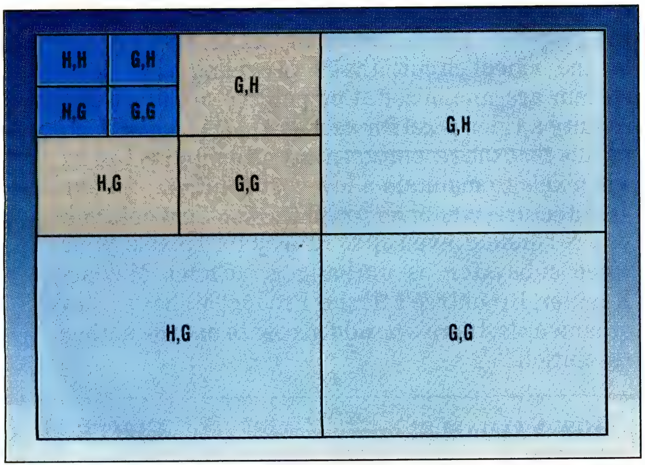
EFFICIENT ENCODING

A technique that more evenly distributes the compression and decompression procedures, dubbed Captain Crunch, was developed by Media Vision, Fremont, Calif. Like MPEG, it's a transform-based algorithm. Unlike MPEG, it combines the wavelet transform, frequency-based tree encoding, and quantization techniques for efficient bit-rate control. The wavelet transform was chosen because, among other reasons, it lends itself to extremely efficient hardware implementations. Captain Crunch employs methods of image decomposition that closely mimic the human visual system to obtain efficient representations of the image.

The first two operations of the Captain Crunch compression algorithm, the discrete wavelet transform and the tree-based encode, differentiate it from competitive compression standards *(Fig. 1)*. For decompression, the algorithm is essentially reversed. The orthogonal wavelet transform yields an alternative signal representation that has proven useful in the analysis of multi-resolution image data. Captain Crunch implements a hierarchical wavelet decomposition to pass the input data effectively through a parallel set of discrete-time bandpass filters.

Captain Crunch deals with digitized video signals in the YUV color space. In a compression application, the video signal is convolved with a wavelet transform to produce a series of coefficients that are more compressible than the original data. The wavelet travels through a pair of filters known as the quadrature mirror filters, which consist of a high-pass filter G and a low-pass filter H. The two filters form a complementary pair that split the input signal into two half-band output signals that are then subsampled by a factor of two *(Fig. 2)*. The splitting process continues until three octaves are created.

The algorithm's tree-based encoder locates and transmits information about image features, such as edges. First the low-resolution sub-bands are processed, followed by successive higher-frequency bands. The computed image data is evaluated against previous frames in the wavelet domain to determine any differences. A decision must then be made to either send the data that's changed, send all new data, or copy the old data.



2. In the Captain Crunch compression algorithm, two filters—G and H—form a complementary pair. They split the input signal into two half-band output signals. Those outputs are then subsampled to generate the high- and low-pass bands.

Because the human eye is less sensitive to high-frequency data, a simple quantization method is used, whereby higher-frequency data is quantized more than lower-frequency data. Hence, the compressor can quantize the high frequencies more without a perceived loss in quality. The quantized data is sent through a Huffman encoder to obtain a more uniform probability distribution. The resulting data is the compressed data stream and tokens, which tell the decoder what to do with the data streams.

REAL-TIME OPERATION

Another important compression-decompression scheme is Indeo. Developed by Intel Corp., Santa Clara, Calif., Indeo allows video to be captured and compressed in one step as it's being recorded in real time. Running on a video-capture board, Indeo compresses a one-minute (50-Mbyte) video clip captured in a 160-by-120-pixel window down to 9 Mbytes. Compressible video windows can be up to 320 by 240 pixels at speeds up to 15 frames/s.

An advantage of Indeo's real-time capture and compression is that when recording, no video frames will be dropped or lost as the CPU and hard-disk drive try to keep pace with the incoming uncompressed data. As a result, all data will be available later if a higher-quality playback is desired.

Indeo employs both lossy and lossless compression techniques. The overall compression ratio depends largely on the type of information contained in the file. Processes are executed by the Indeo algorithm include color subsampling, pixel differencing, run-length encoding (RLE), vector quantization, and variable-content encoding (VCE).

Color subsampling, as performed in Indeo, is a lossy compression technique that reduces data by lowering the color depth of each pixel. To do this, it averages the color value across a group of pixels, rather than keep each pixel's full-color depth. This is effective because the human eye is more sensitive to changes in brightness (luminance) than color (chrominance).

Once the composite analog signal is digitized, all of the pixels are transformed into a format made up of Y, U, and V planes. The Y plane contains the brightness data, while the U and V planes hold the color data. Using groups of 16 pixels, color subsampling doesn't alter any Y data, but requires just 8 bits to describe the color information for all 16 pixels in both the U and V planes. This process effectively removes details that can't be seen by the human eye while reducing the pixel color depth from 24 to 9 bits/s.

After subsampling, pixel differencing comes into play, in which successive frames are compared. Because the background data tends to remain the same, many pixels can be eliminated. The RLE lossless technique looks for continuous runs of pixels that all have the same color values. RLE is only employed when the pixel differencing scheme can't eliminate any pixels. Compression is achieved because RLE only needs to encode a value of zero and a count of how many times to repeat it.

There are some areas where RLE can't be employed because adjacent pixels are similar but not identical. Here, Indeo employs vector quantization, a lossy scheme, to find values in which the differences aren't that great. Those values are then grouped together and assigned an approximate value from a precomputed list.

Indeo's VCE supplies the final stage of lossless compression by encoding chunks of information that vary in size with a fixed number of bits. Compression is achieved when large chunks of data are found that can be encoded by this constant bit length. The technique also helps the host CPU accelerate video playback during the decompression process. The CPU can quickly reconstruct the image from this uniform bit length, rather than continuously manipulate different bit lengths from the compressed stream.

To work with the Indeo architecture, Intel offers its i750 family of video-processor chips. The 82750PD supports the real-time, single-step compression needed to create Indeo video-format files. In addition, the processor is reprogrammable, meaning that users can upgrade their systems by loading the new algorithms as they become available.

MAINTAINING QUALITY

In applications like CD-ROM-based video games, one of the biggest concerns is maintaining high-quality video, rather than how long it takes to compress the video signals. This led to the development of a fourth compression-decompression scheme, Cinepak, which employs a technique called vector quantization. Like MPEG, vector quantization is highly asymmetric, meaning that it takes much more compute power to compress the data than to decompress it. But, also like MPEG, once the data is compressed, a very simple process or simple hardware can handle the decompression in real time.

Cirrus Logic, Fremont, Calif., a licensee of Cinepak, offers a series of ICs that feature a data rate of 24 frames/s with resolution similar to MPEG. The company supports the scheme throughout its graphics product line. "By licensing the technology, we can build the codecs directly into our drivers right off the bat to supply accelerated playback," says Philip Bernosky, a business marketing manager at Cirrus Logic. "Hence, our customers don't have to build a generic interface. When the codecs are built right into the drivers, we can write directly to our frame buffer."

While the compression scheme chosen is a make-or-break decision, the way that the video capture front-end is implemented also becomes important. Although the quality issues of video playback focus on frame rate and resolution, the capture portion deals with the synchronization, color separation, and scaling tasks required to convert an analog composite-video waveform into a digital video format.

One particular low-cost video-capture processor that delivers scaled digital video from an analog NTSC or PAL source comes from Brooktree Corp., San Diego, Calif. The Bt819 processor, which sells for $17 in large quantities, integrates analog-to-video converters, DSP technology for the synchronization and color separation, and a comprehensive image scaler. As a result, it can deliver a digital video stream scaled down to any arbitrary size below full resolution.

ALLOCATING BANDWIDTHS

In systems that integrate video and graphics using a unified frame buffer, a key to the architecture is the ability to allocate the memory-interface and system-bus bandwidths. The Bt819 accommodates this by supplying a temporal decimation control for the video stream. As a result, the frame and field rate can be throttled before being fed into the frame-buffer controller. By reducing the video-stream bandwidth in the time domain to under 30 frames/s, the video requires less bandwidth.

The Brooktree architecture is complementary to MPEG and to software codecs like Indeo and Cinepak. With either method, the host CPU can single-handedly manage the decompression, but only in a small window. If the window is scaled up, the frame rate and color quality both drop. Brooktree's hardware scaling requires that the host CPU just process the number of pixels contained in the original file size. That window is interpolated and scaled up in hardware so the image can be displayed at any size without any performance loss.

Brooktree's architecture is unique in that it employs a video cache that shrinks the frame buffer, lowering overall system cost. This is accomplished by enabling asynchronous loading of the video with the graphics. Hence, the bandwidth requirements of the video circuit that's providing the video stream are minimized. Competitive architectures require a video pixel for each graphics pixel, which means that the resolution must be limited to 640 by 480 pixels to maintain a low-cost solution. "In our architecture, whatever graphics display resolution you're running, even up to 1280 by 1024 pixels, your video subsystem is unchanged," claims Michael Kastner, Brooktree's Senior Product Manager. "In other words, there's no added cost to use the higher resolution."☐

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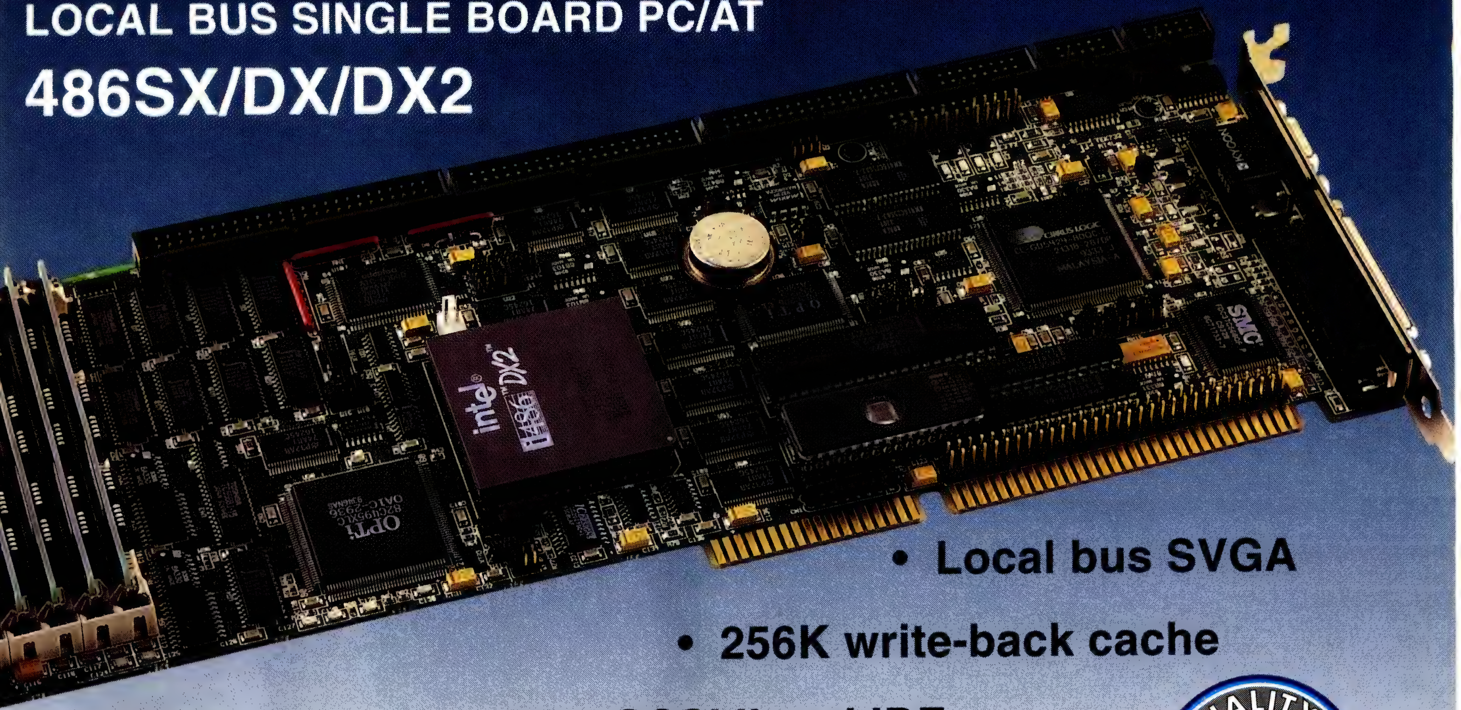

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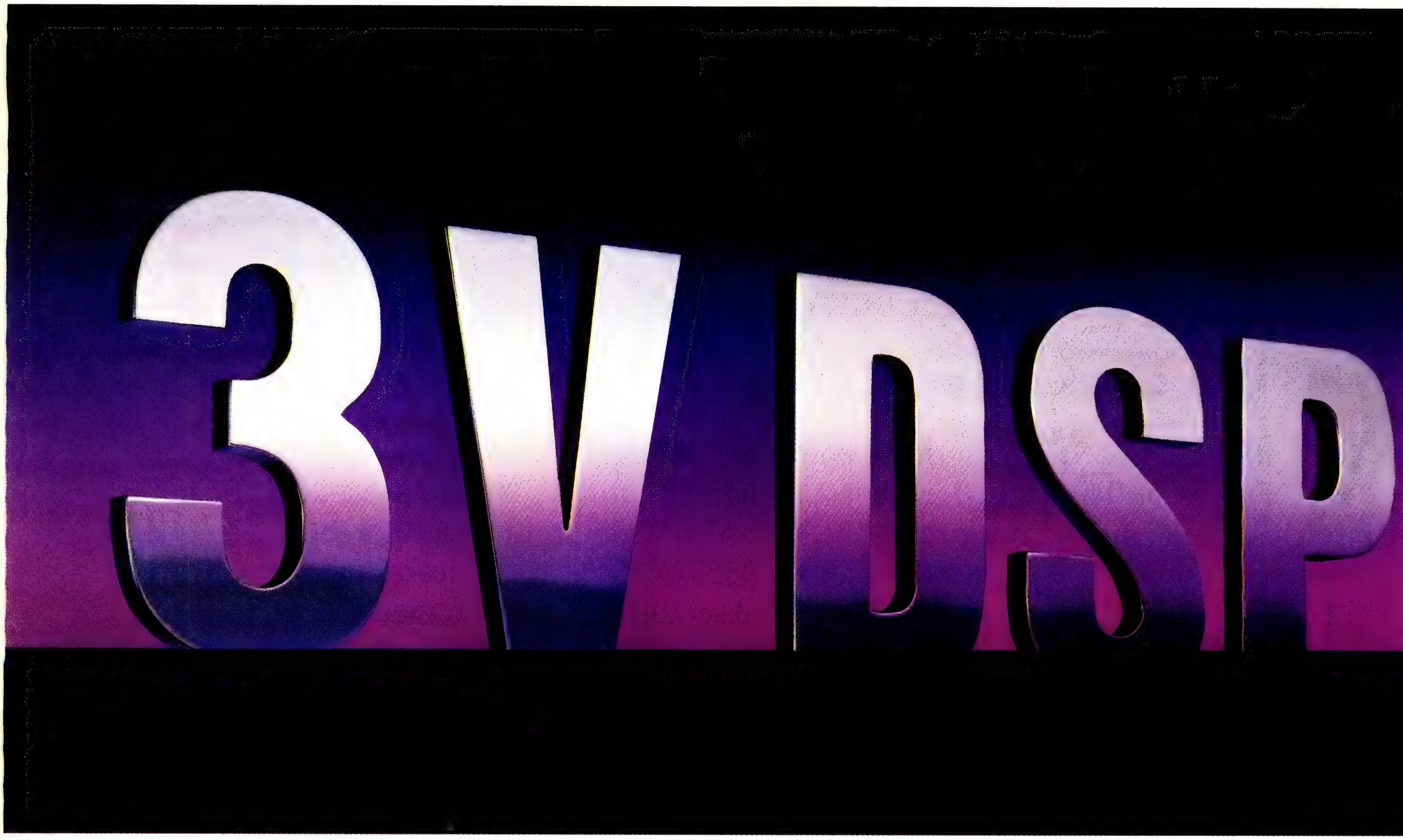

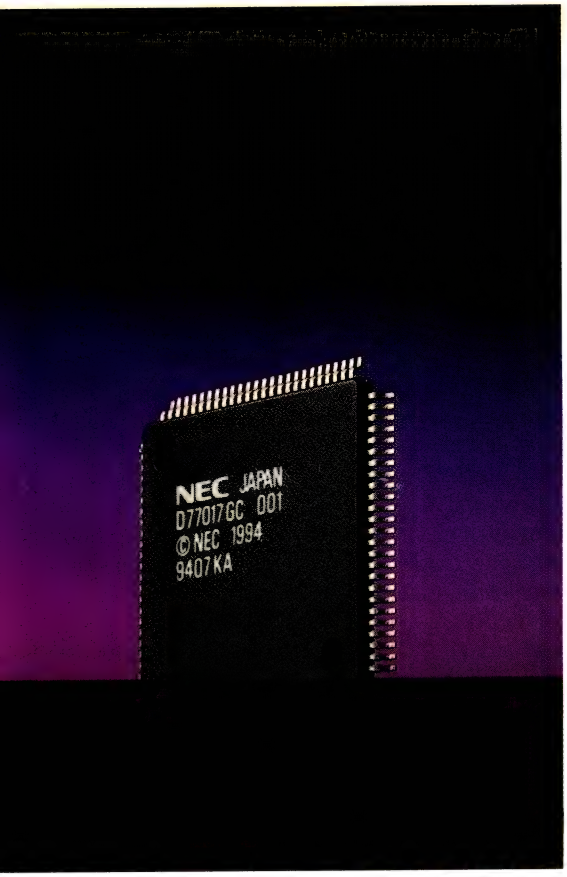

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READER SERVICE 129

STREAMLINE YOUR DESIGN PROCESS WITH QRPD

FOLLOW THESE GUIDELINES AND YOU CAN OVERCOME THE SEVEN DEADLY SINS THAT PREVENT QUALITY RAPID PRODUCT DEVELOPMENT

ORION KOPELMAN
Global Brain Inc., 555 Bryant St., #210, Palo Alto, CA 94301-1704; (415) 327-2012

Not long ago, Xerox used 600 engineers to design a 50-page/min. $150,000 color printer in only three years, while the previous black-and-white project took them over six years to complete. Why can some companies consistently reduce time-to-market and not others? Which new practices allow a company to drastically reduce development times and costs? Does one management methodology work better than another? Will it work effectively for different size organizations?

Many companies haven't found the willpower and determination to implement the fairly well-known techniques advocated by Quality *Rapid* Product Development (Q*R*PD). Old habits keep them chained to past modes of operation. The most common malignant practices in the technology-driven industry that cause this are called "the seven deadly sins" that prevent Quality *Rapid* Product Development. The leadership solutions presented here are their remedies.

Compared to several years ago, most new-product development projects run on schedules that now span only one year or less. Estimates say that collective human scientific and technological knowledge doubles every year and a half, and may double annually by the year 2000.[1]

Most technology management at least acknowledges this challenging environment. Some companies have adjusted and even thrive on it. However, bad habits have kept most companies stuck in the past. *Business Week* (Aug. 16, 1993) recently reported that 46% of all R&D money spent in the U.S. goes to what eventually becomes a product flop. This means that almost half of our well-intentioned, hard-working engineering effort results in much ado about nothing. The story focused on many reasons, including marketing strategy. Nonetheless, most agree that the single greatest factor remains the ineffectiveness of the new-product development process—particularly, how to choose the right product to develop, and how to get it to market in the shortest possible time. When we don't, the results to our companies' financial health can be quite harmful, or even fatal.

Responding to this adventurous, "survival-of-the-fittest" global technology race of the 1990s, many companies have begun using the Q*R*PD management methodology to develop products in up to half the time.[2] First developed in the 1980s, Q*R*PD sprang from a conglomeration of theories and techniques experimented with by various organizations of all sizes, from startups to global giants. By distilling the methods and management wisdom that proved most successful, it attempts to provide a synthesis of the best practices for the 1990s and beyond.

In the 1980s, many high-technology companies enjoyed fantastic and sometimes overnight success. In the 1990s, though,

TABLE 1: OVERCOMING QRPD HURDLES

Sin	Remedy
1. Trying to do too much in one project.	USE INCREMENTAL INNOVATION.
2. The NIH—Not Invented Here—syndrome.	INNOVATE RATHER THAN INVENT (RE-PACKAGE).
3. Not everybody buys-in to a common product vision.	REDO "SSSS" NEGOTIATION.
4. Functional organizations refuse to relinquish control to project teams.	GET TOP MANAGEMENT TO BUY INTO Q*R*PD.
5. A weak project team leader, or one that lacks authority.	SELECT CAREFULLY, AND ANOINT RESPONSIBILITY TO.
6. A poor product development process, or none at all.	WORK ON THE PROCESS AND PRODUCT SIMULTANEOUSLY
7. No *"Chicken Test"* on a working prototype early in the schedule	DO IT!

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as the market matured, superior quality and high productivity are the admission price just to compete.

Hence, the "Q" in Q*R*PD: Keep quality first in mind. This means giving customers value.

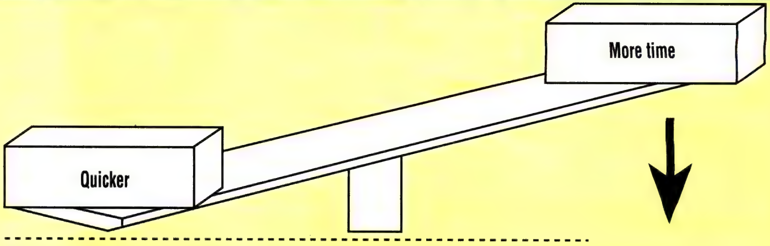
The emphasis, however, now shifts to attaining quality much more rapidly. Concerned with national economic competitiveness, Ron Brown, U.S. Secretary of Commerce, noted at the first government-industry Technology Summit (November 1993), "An age in which change is the only constant requires unflagging, sustained (quick) innovation." To survive in a leapfrog world, where even current products are here today and obsolete tomorrow, every project must turn into an overnight successful new product. Q*R*PD recognizes that time is of the essence.

Using Q*R*PD-like techniques, many companies have accelerated product development times by up to 50%, with lower overall spending levels. Examples include Xerox, who reduced their average time-to-market companywide by 50% (on comparable products), with 50% less engineering resource dollars.

Management expert Peter Drucker reports that Toyota, Nissan, and Honda now bring out a new automobile model in only 18 months.[3] U.S. car makers have achieved a three-year cycle, down from five a decade ago. Intevac, a mid-sized company in Sunnyvale, Calif., completed the latest molecular-beam-epitaxy machine for depositing gallium arsenide on semiconductor wafers in eight months instead of the usual year and a half. Rolm, a Siemens Company, developed a certain genre of voice-mail products in successive cycle times of four years, two, and currently one.

One can deduce that because the team sizes stay about the same, no matter how long the project lasts, most companies have spent less money by developing products in up to half the time. Consequently, there was greater returns on their investments. John Young, retired CEO and president of Hewlett-Packard, remarks that, "improved new-product development cycle time is not only free, it's profitable. It doesn't cost you anything, it's more fun for everybody, and you do it right the first time!"

TABLE 2: SEE-SAW SCHEDULING AND SPECIFICATIONS (SSSS)



Marketing & Management
"We need it within X months or else?"

1. Window closes
2. Can't predict market
3. Competition kills
4. Can't pay salaries anymore

Technical Team
"What's-the-earliest-date-by which-we-can't-prove-we-won't-be finished?"

1. Evaluate risks, iterations
2. Each member commits to own schedule by subsystem (prays)

Q*R*PD facilitates this by combining the best of both startup and larger, more mature company environments. We've all heard and seen the swift successes achieved by many booming startups. They took advantage of flexible, fast-paced, free-wheeling, entrepreneurial innovation. This spirit contributed significantly to Silicon Valley's mushrooming, and to that of other technology hotbeds around the world. And yet many of these companies lacked the staying power to turn in repeat performances. They subsequently disappeared or declined almost as quickly as they appeared.

On the other hand, larger, more stable companies have suffered from stagnation and product development cycles that have slowed to a crawl, relative to the industry as a whole. Nonetheless, some of these giants developed some structure necessary for every company's growth and long-term success in today's global technology race. Q*R*PD blends the best of the startup and large company practices, thereby adapting to changes occurring at an accelerating pace around us, and delivering quality new products just in time.

However, habitual ways of doing things have kept companies that have not implemented Q*R*PD chained to their past modes of operation—as their once full coffers dwindle further and further. To break those chains, they must overcome the seven deadly sins of Q*R*PD *(Table 1).*

The first two "sins," *Trying to do too much in one project*, and *The NIH—Not Invented Here—syndrome*, often go hand in hand. NIH refers to the tendency of technical people to think they can come up with a better design themselves, even at the expense of not having a justified return on investment for their company. By not using technology available from previous projects or from the outside, one creates a monster-size endeavor. These "megatrap" projects are rarely completed on schedule.

For example, in the mid-1980s, a California company spent five years and $15 million to develop a pc board that fit into a slot in a personal computer, and provided 10 Mbytes of hard-disk storage to the then floppy-only systems. They developed their own firmware and an electronics board—a thin hard disk that fit in one slot in the PCs.

A competitor decided to buy a commercially available 20-Mbyte hard disk that took up one and a half slots and mated it to an off-the-shelf controller card. By just writing some firmware, they managed to spend three months, $100,000, and ship a product with double the capacity for the same price, ahead of the first.

More recently, NASA and McDonnell actually developed a prototype of a reusable rocket, the Delta Clipper, on schedule and within budget—18 months, $60 million (a recent redesign of the space shuttle's toilet cost taxpayers $23 million). They achieved this by using "hand-me-downs," a guidance system from an F-15 jet fighter, and some leftover fuel tanks from another program.

The rocket flew successfully in the summer of 1993, and restores hope to the U.S. for a viable commercial space launching program that competes

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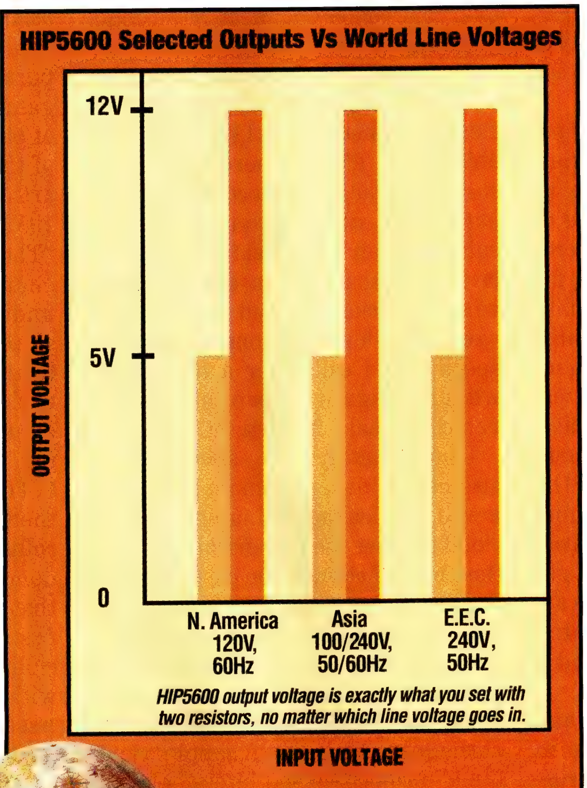

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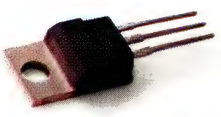

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with the French Ariane and the Russian Proton.

The solution to avoiding these two sins lies in recognizing that particularly in the 1990s, we must become incremental innovators, rather than inventors. Innovation can be defined as introducing novelty (new know-how) into practical use (technology) to increase the customer's value and satisfaction obtained from the seller's or manufacturer's resources. Lots of technology already exists, though untapped, and more is being invented at an alarming pace. The U.S. issues over 300 patents each day. Over 200 million scientists and technologists go to work every day—more than the number of people that lived on the whole planet 2000 years ago. Why not package available inventions as a subsystem in your product? There's plenty of profit margin for all, if you find the right application.

Furthermore, you must become adept at playing the game of completing as many development cycles as possible, each one resulting in a salable, desirable product. This incremental approach means swinging for base hits. Sometimes singles turn into doubles or triples... or even home runs. By introducing successive generations regularly, a practice perfected by many Japanese companies, you can lower overall risk while learning more about the market and the technology, and continuously refining your products. Best of all, you rarely strike out completely, and always get paid by the customers along the way. They win, too, because you presumably provide them with value and a better way to do something.

Even engineers, marketeers, and other project team members win in the long run as their companies prosper. But management must steer technical people clear of their natural propensity to want to invent everything by themselves, and marketeers from wanting to have everything ready for the product that "must ship next month." NIH takes on many insidious forms, including creeping elegance (wanting to do it perfectly to show-up the others), and pride-of-ownership issues. For example, a top-notch, senior software engineer, working on a Motorola 68000 platform, was recently doing object-oriented code for the first time. He claimed it would take him longer to bring several helpers up to speed than to do it all by himself. After they were added (the project had plenty of money, not time), he agreed that only now was there a reasonable chance of actually making the aggressive schedule.

Technical people usually underestimate the number of unknowns that arise during the development process. So it's best to categorize each innovation as minor, medium, or major risk, and carefully justify its benefits and return on investment. By combining minimal invention, taking advantage of existing technology, and introducing a limited number of innovations, everyone comes out ahead on an ongoing basis.

To successfully innovate incrementally, the company must agree on a clearly defined, limited set of product objectives. That's where sin 3—*Not everybody buys-in to a common product vision*—comes into play. This results in either technical failures or delays. For example, in one company where marketing and engineering were at odds with one another, a specification called for a quick two-week redesign of a door on an armored vehicle to make it "airtight."

Unfortunately, the specifications also called for a maximum rate of allowed air leakage. Engineering decided to meet the numerical specification, and, of course, the customer had expected "air-tight" to mean zero leakage (required for chemical warfare, especially). The company eventually sent a team halfway across the world to retrofit a totally new design at the customer's site. A simple "slam-dunk" project turned into an eleven-week fiasco.

The obvious, but seldom-followed remedy involves getting the whole project team together to hash-out a written one-page vision. What's required is a careful balancing act of See-Saw Scheduling and Specifications (SSSS) *(Table 2)*. Everyone must participate in a negotiation process of trading off product features, benefits, and costs for the resulting amount of time and budget required for design and production. The goal is to have all team members commit wholeheartedly and knowingly to a set of milestones that delivers a product to the customers and makes financial sense for everyone. Total buy-in assures Doing It Right the First Time (DIRFT), rather than the second or third time.

Next, consider sins 4 *Functional organizations refuse to relinquish control to project teams* and 5 *A weak project team leader, or one that lacks authority*. Management experts have touted the concept of organizing companies along the lines of project teams since the beginning of the Space Age. In one of the first articles on The Project Manager, in 1959, Paul O. Gaddis warned that, "The United States today faces the enormous problem of how to regain undisputed technological leadership... Advancement... will shape our future and determine our survival or extinction... The role of project management will be challenging, exciting, and crucial."

This rings as true today as it did then, yet many functional managers refuse to give up control over their domain. Managers must recognize that their workers' loyalty must lie first and foremost with small interdisciplinary project teams chartered with developing a product rapidly. Association with such departments as marketing or quality should become secondary. Fostering this kind of spirit of commitment to a project will yield remarkable results.

Recently, a 30-year-old company experimented with this concept. They broke off a small, crack team of six people. As a supplier of phone equipment in years past, their bureaucratic, ingrained, and functionally managed organization had earned them AT&T's Quality Leadership Program (QLP) award. However, it also had slowed new product development to a

TABLE 3: SKYROCKETING COST OF ENGINEERING CHANGES

(major electronics products)

Time of design change	Cost
During final production	$10,000,000
During test production	$1,000,000
During process planning	$100,000
During design testing	$10,000
During design	$1000

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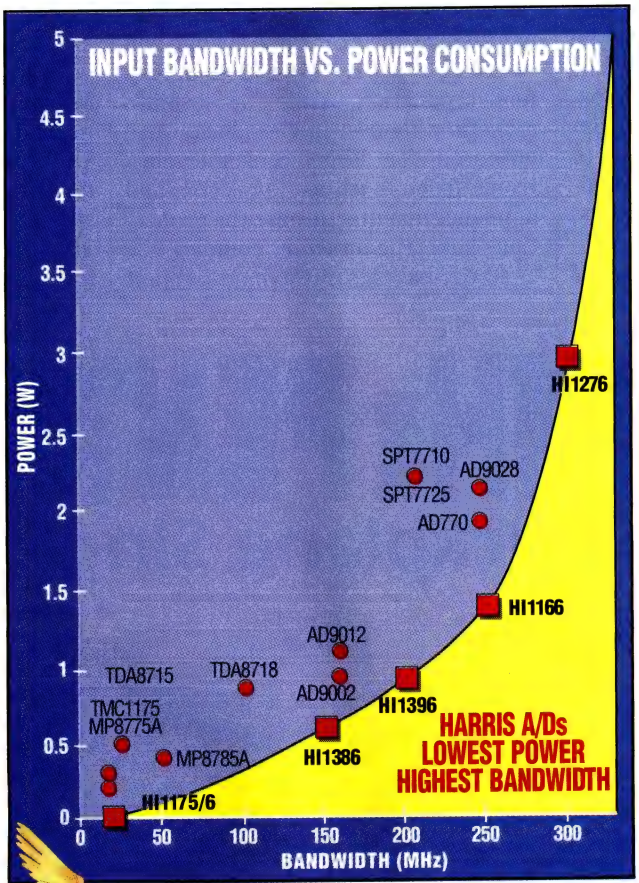

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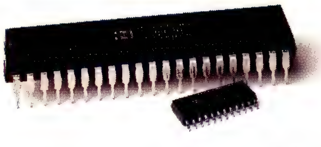

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crawl, by 1990s' standards. The results of their latest project, however, was nothing less than outstanding. They saved a large customer's business and shipped a new product in nine months. This product went into production at the same time as a previous one with an almost identical component count—that project began nine months earlier and met its schedule using standard procedures. The new approach had provided conclusive proof. The project was done in half the time—9 months instead of 18. Gordon Simmons, the project leader, and a graduate of the QRPD training program says, "At times, we ran counter to the accepted norms of doing things, but we met all expected customer deliverables. We could easily do this again and again, if management continues to clear the runway by giving us dedicated people from all departments, and says go!"

TABLE 4: TECHNOLOGY PROCESSES

Maturity level	Characterization
1. Initial	Ad hoc/chaotic
2. Repeatable	Intuitive, depends on individuals
3. Defined	Qualitative, independent of individuals
4. Managed	Quantitative, measured
5. Optimizing	Improvement fed back continuously

Fortunately, reorganizing lines of responsibility into these kinds of project teams doesn't degrade product quality—it improves it. We can see why when we examine the cost ramifications of engineering changes *(Table 3)*. It's clear that the average cost of a change in the design increases tenfold at each later stage in a project.[4] For example, a change during the design phase may cost the company $1000, but that same change will debit the company $10 million during final production. While the absolute monetary figures in the chart were gathered for large consumer-electronic firms (such as TV, VCR, and appliance manufacturers), the proportions hold true for every company.

To combat this, if top management truly buys into QRPD, they will encourage functional managers to release their workers to the project teams early on in the development. Getting all departments involved together, from the beginning, minimizes unforeseen risks. This subsequently prevents tardy changes that cause quality problems, astronomical costs, and time delays.

As a consequence of the layers of entrenched functional middle managers, often the wrong project leaders get selected, or don't really have the authority to accomplish their mission. For example, a company making a linear accelerator for cancer therapy with digital control and a computer interface chose, by default, the engineering manager as the team leader. Unfortunately his lack of experience in linear-accelerator technology resulted in the end product not meeting specifications, four years of development instead of three, and a project

that came in 50% over budget.

Similarly, a company making lasers to correct far-sightedness had three people periodically assume the role of project leader. None agreed on an overall approach or schedule. Worse, none of them had overall responsibility, so they missed identifying the major hurdle on the project: insufficient software resources (the area of least innovation on this project, but still highly time-consuming). The project was shipped in 12 months instead of 9, ironically two months after a competitor introduced a comparable product.

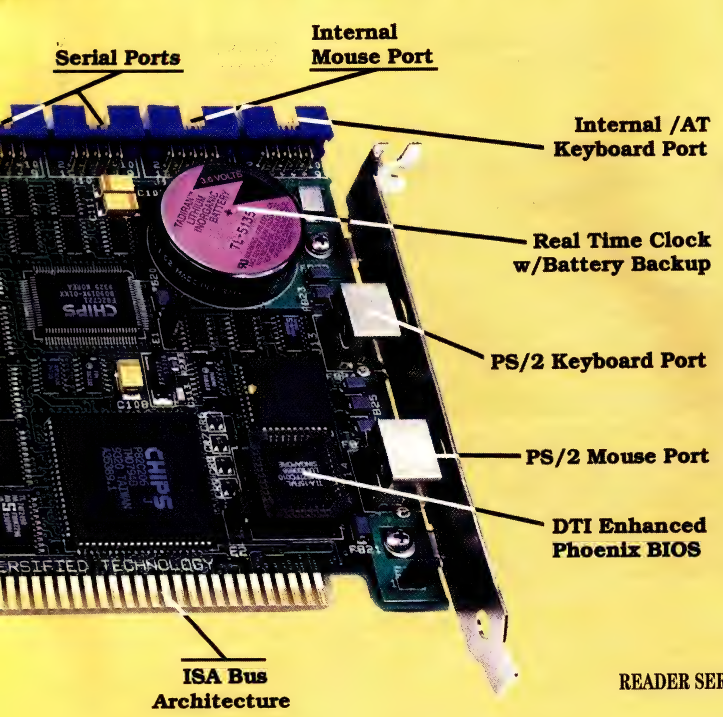
Top management must take the initiative to come up with a matrixed, project-oriented organization chart; assume the burden of choosing the right team leader; and give them the authority needed to meet their huge responsibility.

This includes assigning dashed-line reporting of the team members to the project leader. Consequently, the leader will exert heavy influence on the individuals' performance reviews, and have a better chance of pulling off the project on time.

Obviously, many reasons account for the selection of an insufficiently capable, weak project leader. While many managers do things right, only true leaders will do the right thing. Seen in that light, "Of all the decisions management makes in managing accelerated new product development, none is more crucial to success than the choice of a team leader. A strong leader will be able to overcome many other shortcomings and imperfect management decisions, but a mediocre one will be stymied even by small obstacles."[5] So find an obsessed leader that's confident (and honest), technical, a model worker, a people person, and has high standards and management ability. Then formally announce his/her vital role to everyone that must help on the project.

Sin 6—*A poor product-development process, or none at all*—is an area where most companies fall short. The Carnegie-Mellon Software Engineering Institute has observed five maturity levels in the software development process *(Table 4)*. However, these levels can apply to many types of processes, including new product development. The majority of manufacturing organizations operate between levels four and five—they have streamlined production. Unfortunately, an educated guess predicts that over half of project development efforts utilize levels one or two, about a quarter reach level three, and maybe 10% operate at levels four and five. The last group are usually highly successful companies. Many companies at levels three and above create and use a guidebook. Much like cookbooks, these serve to more predictably follow the recipe every time (even master chefs use them, then improvise on the fly). While never assuring success, it does increase the odds of developing quality new products quickly.

A level-two company with a repeatable but not yet defined new product



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development process can do many things right and still fall into trouble. For example, one company developed a balloon catheter designed for coronary angioplasty, with a potential gross yearly sales of $100 million over a two-year window. Despite use of a corporate plane, the project stalled while transferring it from California's engineering group to the manufacturing plant in Mexico. Production people only voiced concerns after equipment had arrived, not early on in the project. The lack of a well-defined process resulted in a three-month delay that cost the company about $5.6 million in lost profit.

Many companies, cognizant of the ills of such painful lessons, are working hard to leap up the maturity scale. ISO-9000, the emerging international quality standard, and market pressures, now mandate greater emphasis on a continuous process improvement effort. As organizations of all sizes and ages scramble to shake up their perhaps once adequate ways, only the swiftest to mutate survive. One such company, Avantek (currently a division of Hewlett-Packard), has been a leader in microwave electronic components for over 20 years.

However, it lost its competitive edge mainly as a result of slow time to market. Consequently, the company set out to change its basic culture, and established a New Product Process (NPP). Tina Ohlhaver, the R&D Productivity Manager, says, "Q*R*PD identified the common success factors, which maximize the probability of a successful product introduction. After implementing our NPP, with Q*R*PD as a key component of it, we saw an improvement not only in the timeliness of new product development, but also in the excitement and pride the participants in the process felt."

Many others are doing the same thing. EO, now a medium-sized company owned by AT&T, produces both pen-based hardware and software (after acquiring GO Corp.). Only recently a fast-paced, highly entrepreneurial startup, the company's growth led to its asking it's v.p. of engineering to synthesize a company-wide set of procedural guidelines to standardize product development. While eager to accomplish this, the company encountered the standard problem of not having the time to sharpen the axe when so much wood needed chopping soon. Nonetheless, rapidly expanding, successful companies like EO have learned to emphasize equally, and work simultaneously on, both the development process and individual product projects.

The final sin, sin 7, states *No "Chicken Test" on a working prototype early in the schedule.* Every project undergoes a critical test, which serves as a reality check. It finally tells us if the essential technology actually functions as it should. This is called the Chicken Test.[6] It gets its name from tests performed on airplane jet engines. Namely, in order to ascertain that during flight the en-

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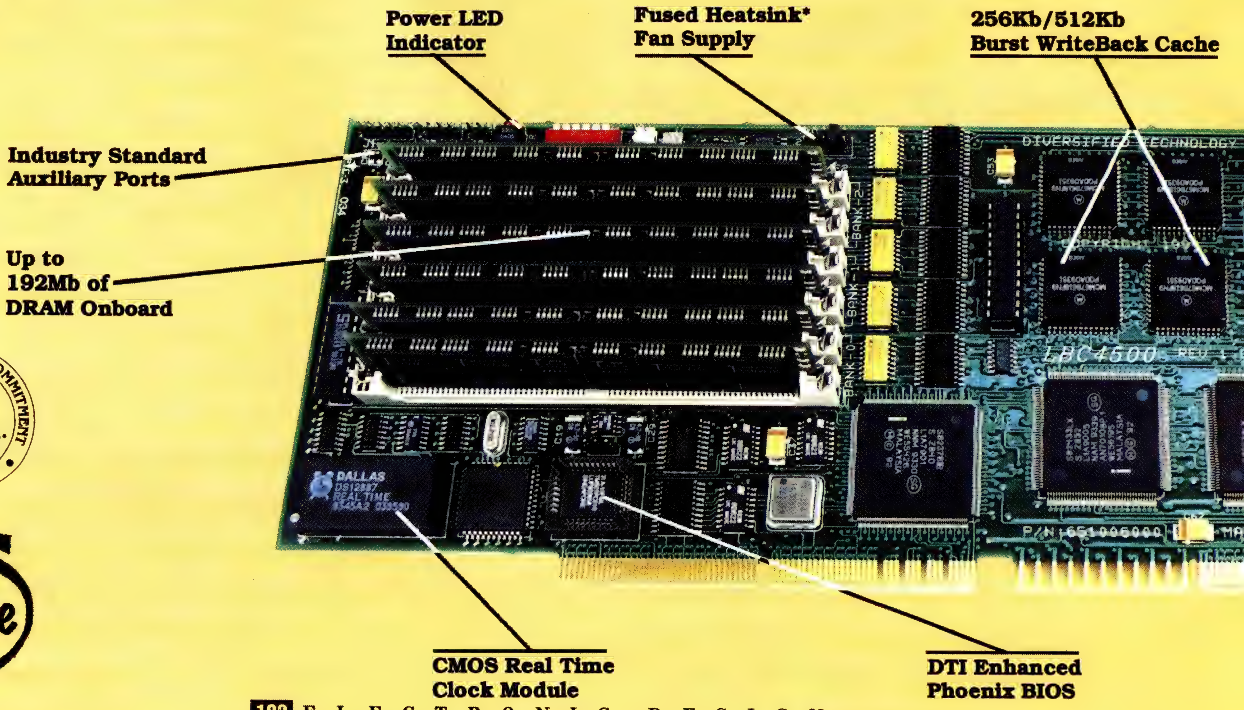
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gines can contend with the ingestion of flocks of birds, a barrel gun several feet in diameter fires live chickens at them. This serves as an early-warning system to uncover a possible fundamental flaw in the design, before spending the whole $250 million necessary to develop a new engine. Every project must eventually undergo and pass a chicken test before it can really take off.

The only question is how late in the project you discover that you may need to take a different approach. Obviously, the earlier the better.

For example, a major mainframe computer manufacturer decided to repackage its systems into a new market application—telecommunications switching. Nine months into the one-year project, the company attempted system integration for the first time. Unfortunately, many of the mechanical subsystems didn't fit together. Over 180 drawings had to be redone, causing a three-month delay in a highly contested market.

To avoid this kind of late-breaking bad news, you must simply have the courage to spend a little extra time and money early on in the project. Do your Chicken Test on a working prototype (even without having all of the bells and whistles yet) within the first 25% of the schedule.

This way you can find out if you're really on track, confirm many of your high-risk assumptions, and possibly decide to alter your course. With a typical one-year schedule, you could fail the test at the 90-day mark, start over, and still probably ship a product ahead of your competition, who had to do massive rework later in their project.

One last remark about the Chicken Test: The war archives of many companies reveal that on average, from the time you have passed this vital assessment point, you still have about 50% of the project left to do. So don't kid yourself. Plan better, and leave plenty of time for system integration, testing, and debugging.

Sluggish product development can cost companies thousands of dollars in lost profits/day, due to late market entry. Consider the fact that 60% of Hewlett-Packard's revenue comes from new products introduced in the last two years. John Young reminds us that only by intervening early in the development cycle, you can hope to accelerate your time-to-market and remain competitive. This requires an investment in revamping the whole process. To survive and thrive in a leapfrog world, where even current products are here today and obsolete tomorrow, you must learn to develop new products swiftly.

So if you found your sins on this list, confess them and choose to change. Transform your environment into a Quality _Rapid_ Product Development company of the 1990s and the next millennia. Many companies, like yours, already practice acceleration techniques, and routinely develop products in half the time that it used to take them. ☐

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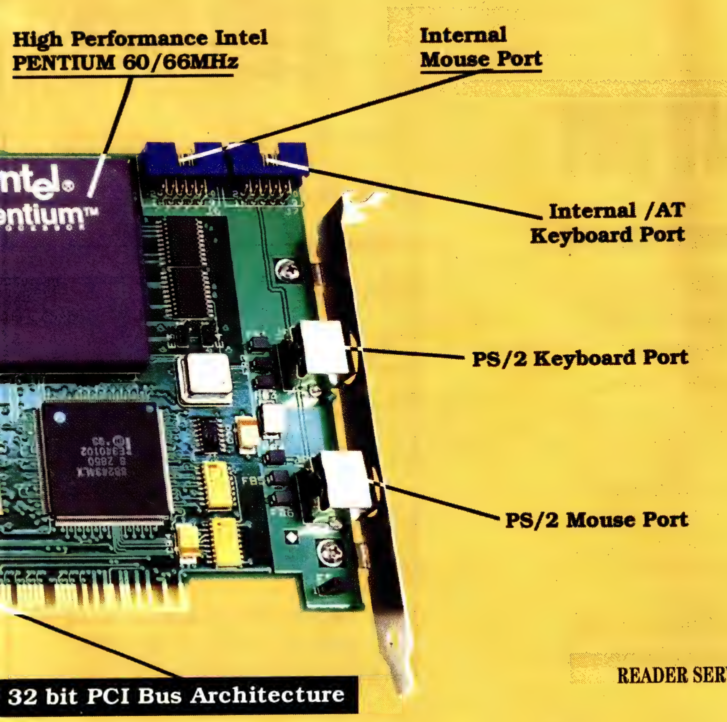

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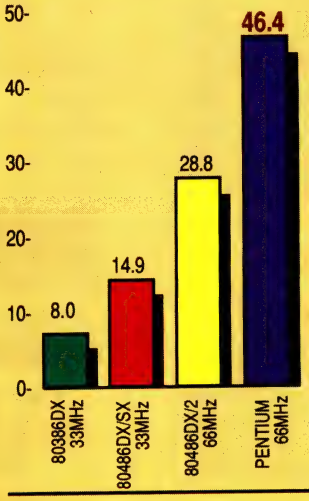

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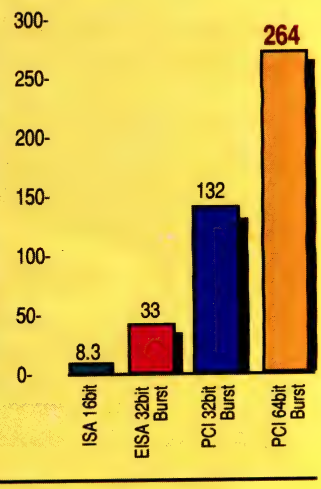

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Orion Kopelman serves as president of Global Brain Inc. His creation of the QRPD methodology is the result of six years as vice president of engineering and cofounder of a division of Mountain Computer Inc. and three years as chairman of IEEE's Santa Clara Valley Engineering Management Society. He holds a BSEE from Stanford University.

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ELECTRONIC DESIGN QUICK LOOK

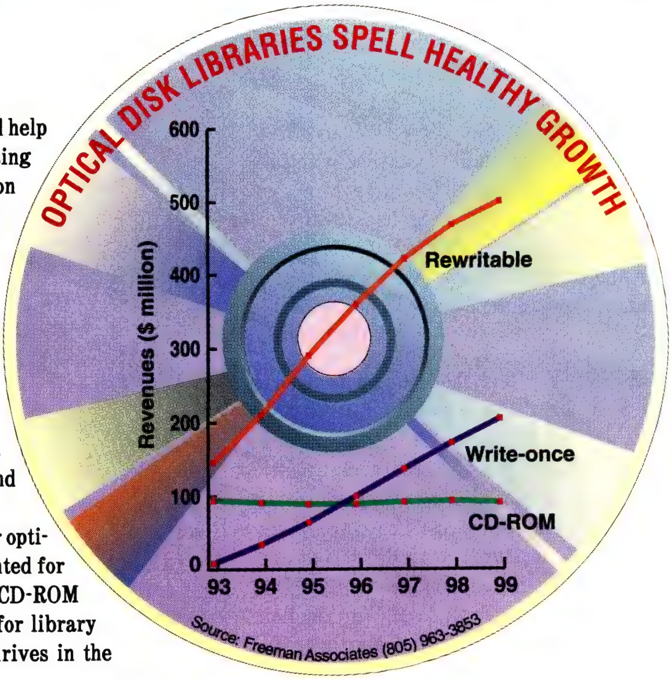
EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Demand for removable mass-storage library devices should help that market more than double in revenues by 1999, increasing from $1.35 billion last year to be worth at least $3.1 billion by 1999. Library media include tape drives, CD-ROM, write-once optical disks, and rewritable optical disks. High-performance units oriented toward mainframe environments have given way to smaller, lower capacity, lower cost versions serving mid-range and network storage requirements. Mushrooming memory requirements across nearly all platforms and applications are driving the growth, say Robert C. Abraham and Raymond C. Freeman Jr., authors of the Freeman Report, *Mass Storage Outlook*.

To meet that demand, library manufacturers are responding with a wider range of technologies and price points, explain Abraham and Freeman, management consultants based in Santa Barbara, Calif.

Rewritable and multifunction devices will dominate the market for optical disk libraries in the 1993–1999 period. Rewritable libraries accounted for 74% of units sold and 58% of revenue last year. A robust market for CD-ROM drives and software is triggering related jukebox offerings. Look for library makers to offer products containing CD-ROM and CD-recordable drives in the same cabinet, according to Abraham and Freeman.


OPTICAL DISK LIBRARIES SPELL HEALTHY GROWTH

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TALES FROM A SKUNK WORKS

Moving beyond technology to develop products exposes your skunk work's team to new corporate traps and pitfalls. Surveys report the biggest obstacle faced in new product development is the firm's own new product development process. Firms are learning that market targeting is paramount. Decades of painful experience are starting to seep through, showing managers that the "better mousetrap" model for new ventures does not work. Customers must buy the product for sales to result.

Unfortunately, in most firms, corporate's reasonable desire for market understanding gets translated into a quest for numbers. That is not how managers approach technology understanding, but they find strange comfort in market numbers. High-tech marketing gurus emphasize that qualitative knowledge is crucial, but the process demands numbers.

Project approval depends on meeting a hurdle rate. "We invest in products that can address markets in excess of $50 million, growing above 30% in five years." Typically a template must be filled out, and approval depends on sufficiently big numbers.

If the market is still emerging and the technology is new, of course, the market reports giving the sizing numbers that your management wants are not yet available. You still have a template to fill out. Doing it yourself presents problems. The market hasn't happened yet, uncertainty is high, opinions differ, and the assessment of the product team might be biased. You decide to hire an expert, but funding is limited because the project is not yet approved. Later you will spend millions, but not now.

Two firms apply. The first is a person between jobs who "knows the market." He will gladly complete the template with whatever numbers are required and sign it.

The second consultant is a pro. He has been in business for years and adheres to professional codes of conduct. He proposes a research project to gain understanding and size the opportunity.

The first bidder promises a completed template in a month for $3,000. The second suggests a monthly retainer, estimating a six-month, $50,000 project. Guess who gets the job?

The decisions made at the concept phase determine 80% of project costs and most product features and specifications. Competitive advantage comes from an early and deep, holistic understanding of market needs, technology, and implementation. This is the best investment you can make.

Typical firms spend 4 to 6% of their budgets at the concept phase, but the leaders spend 15 to 25%. This pays off in shorter cycles, better products, and higher profits. Demand plans, but don't chain your skunk works to trivial templates. You want knowledge and commitment, not superficial numbers.

John D. Trudel, CMC, lectures and provides business development consulting. Trudel is founder and director of The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 640-5599; fax (503) 543-6361; e-mail: JohnTrudel@aol.com.

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Write or phone the company for a demo disk of EasyCASE 4.0 for Windows, Workgroup Edition, which gives concurrent, multi-user access to shared design projects on the network server. At low cost, EasyCASE gives a choice of structured analysis, design and data modeling methodologies: Yourdon/DeMarco, Gane & Sarson, SSADM, Ward-Mellor, Hatley, Yourdon/Constantine, Martin Information Engineering, Shlaer-Mellor, Chen, IDEFIX, and Merise, along with a data dictionary repository. Contact Evergreen CASE Tools Inc., 8522 154 Ave. NE, Redmond, WA 98052; (800) 929-5194 or (206) 881-5149; fax (206) 883-7676. CIRCLE 461

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KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

Thank you, thank you, thank you! Through our shared interaction, I completed the production of 100 Kmet Korner columns two weeks ago. This column marks the transition into the new century. But before moving forward, let me seize this opportunity to take a look back over the past four years.

It took me four years to write 100 columns. The collection contains 45,859 words and 47 illustrations. Each column took about a day to create. As a result, in this particular activity, I produce words at the blistering pace of 458 words per day!

My experiences provide the source material for the column. These experiences occurred in a variety of settings. Getting an EE degree does something to you. Making the push to get an advanced degree while working full time influences your thinking. Working for a large aerospace company and a large commercial company gave me many useful insights. Starting my own business expanded my horizons. But at the base of all this resides the design process—the ability to take something that resides in the mind and through a sequence of transformations make it real.

I don't write this column—I design it. The numbers in the second paragraph shine light on the design process that are often times overlooked. Four years to write 45,859 words? I know, you're thinking I'm not very productive. Well, I've got another bedrock data point on my design process. A few years back I wrote a book titled *New Product Development: Design and Analysis*. It contains 132,000 words and consumed 14 months of my time to engineer it. For this 14-month period, the book was my life. Fourteen months times 25 days per month yields 350 work days. My productivity on this effort then computes to be 377 words per day.

Could these data points be telling me something about the design process I follow? They most certainly are! I can produce finished product made up of words and pictures at an average pace of 417 words per day—not much faster and not much slower. The tools I use (PC or Mac) have little affect on my productivity. My work environment dominates my performance. Put me in a crowd with phones ringing, people talking, PA systems squawking, e-mail coming and going, and I get virtually nothing done. Give me a clean, well lighted, quiet place and I'll average 417 words per day. I know my number and I know the necessary environmental conditions required to achieve it.

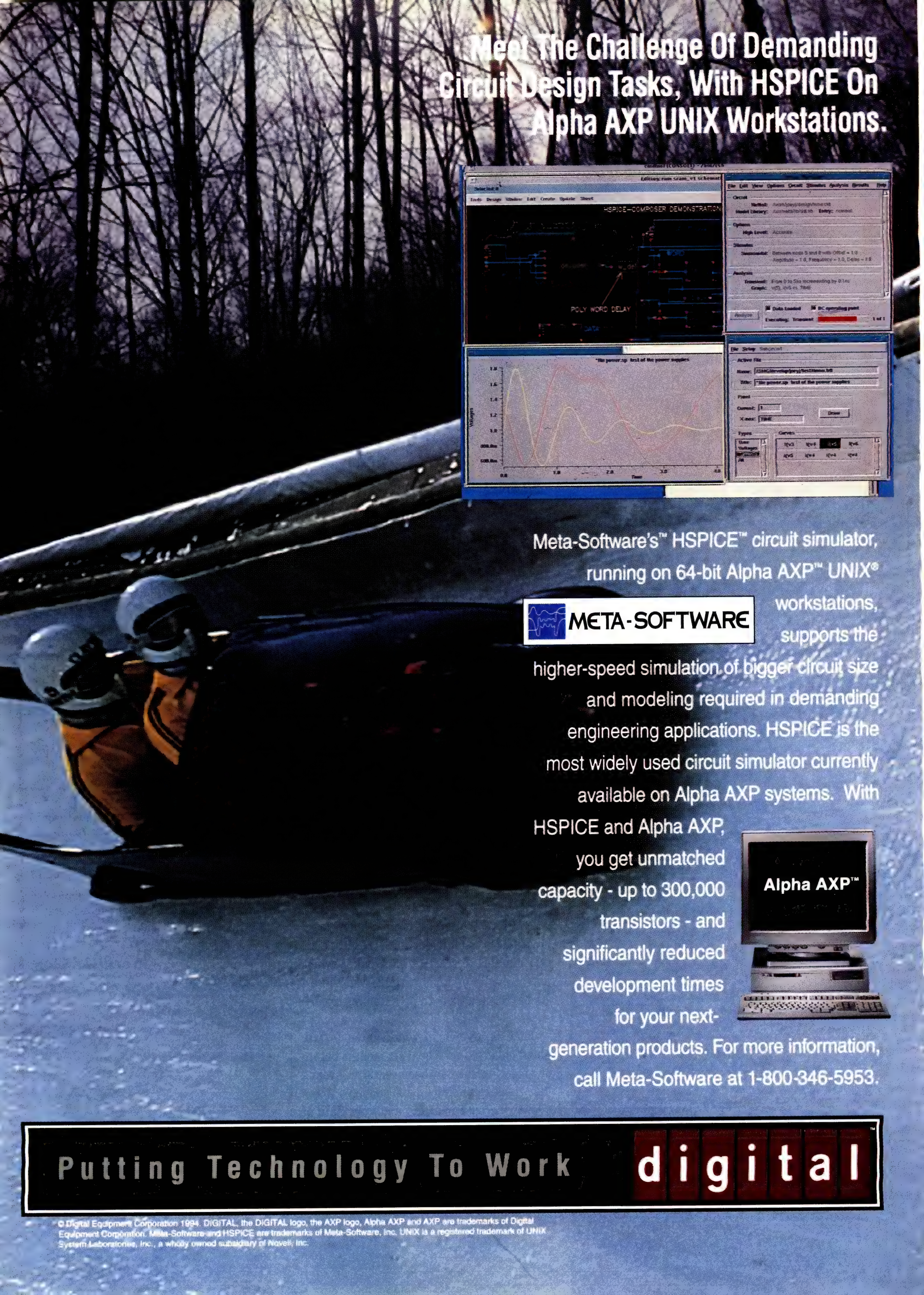
Here's how I put what I know about my design process to use. When a writing job comes in—and most of what I do involves writing—I estimate the number of pages in the job. And guess what? I've refined my skills at page estimation to the point where I can now hit the end result within 20%. Then, based on page count and the conversion factor of 250 words per page, I compute the number of work days I'll need to do the job. With this information known, I then interact with clients and customers to develop a win-win business situation.

My message in this column—learn from the results produced by your design processes. What is the average rate of output they produce? What tools are required to get that rate? What environmental effects are needed?

Go to work on this. As you search for your design process number, you'll have to time travel to the past. Get the data, analyze it, internalize it, and put it to effective use. The more you know the faster you can go!

And once again, thanks for your support over the past four years.

Ron Kmetovicz's The One-Minute Time to Market Self Assessment, which identifies five key behavioral patterns exhibited by fast-moving new product development organizations, is available free to the readers of Electronic Design by contacting Time to Market at the address above.



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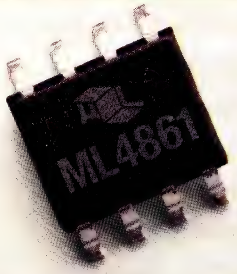

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READER SERVICE 236

MY VIEW

...Huevos rancheros

BY FRANK J. BURGE
Director of Market Development for Electronic Design

Lately I've had more than my share of breakfast invitations and a few months back the invitation was from a new friend who wanted to talk about the networking market. Now I don't know diddly about networking, but the word is out that I'm a pretty good early morning listener. And having breakfast with a good listener is often just the therapy one needs to think through a troublesome problem.

Listening doesn't come naturally to me but is a result of some very good advice my barber gave me more than a decade ago. My barber, who makes the world's best huevos rancheros, has a theory that the person who orders the most food is guaranteed to be the best listener at the table. Think about it. You meet for breakfast and your breakfast partner orders a toasted bagel and a cup of decaf. You order huevos rancheros with a side order of corn tortillas and know you'll have a good listening day. It takes less than two minutes to scarf down a bagel, which leaves plenty of time for talk. And there I sit having another great listening experience.

Back to my friend who wanted to talk about networking. About six months before our meeting she had been recruited from a fast track communications company, given a hefty increase in salary and a sack full of options. Her assignment was to lead her new employer into the networking business, which also involved developing a new channel strategy and the like. At the time she was being courted for the job there were all sorts of management assurances that the company was dedicated to the market and that she would have the budget and top management support to get the job done.

Little did she know that the real assignment was to drag the company, kicking and screaming, into the '90s while fighting senior managers—the resident tree huggers—who just didn't get it. Anyway after six months of fighting City Hall my friend was tired and demoralized by the experience and by management's unwillingness to pony up the money it takes to become a serious player in the market: Play to stay or don't play. Except for a few brief comments to signal that I was following her conversation, my new friend had done all the talking. As I was putting away the last tortilla she asked: "What do you suggest I do?"

I took a sip of tea and replied: "Get a new job." Two weeks ago I got a nice note thanking me for that breakfast meeting three months ago and the news that she had taken my advice and had accepted a new job with the market leader. Huevos rancheros work magic. Unfortunately, my friend's experience is not that uncommon because there all sorts of companies out there that are restructuring to position themselves to be more competitive in the emerging growth markets or reengineering the organization in order to survive.

But many of those companies are just going through the motions, playing the latest restructuring tune. Behind the facade nothing much is changing because management isn't listening and particularly unwilling to listen if the bearer of the strategy is a young, articulate, and aggressive woman. Now that's nutso, especially when the young woman has more market savvy than anyone in the organization. Time for management to take a breakfast break. Order up the huevos rancheros.

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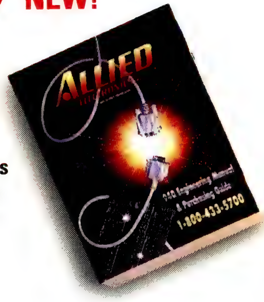

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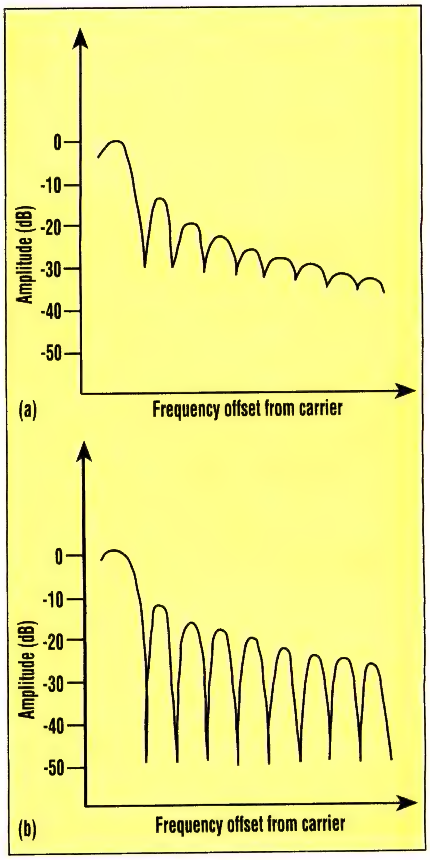
Usually, symbol mapping accuracy and carrier suppression strongly depend on bias amplitude, dc offset, and pulse rise/fall times of mixer-driver signals. In addition, the mixer itself introduces distortion due to hybrid imbalances and dissimilarities in the diodes.

Figures 2a and 2b illustrate the influence of drive-circuit performance on the resultant mixer output spectrum, using a deficient driver *(Fig. 2a)* and the optimum mixer driver described here *(Fig. 2b)*.

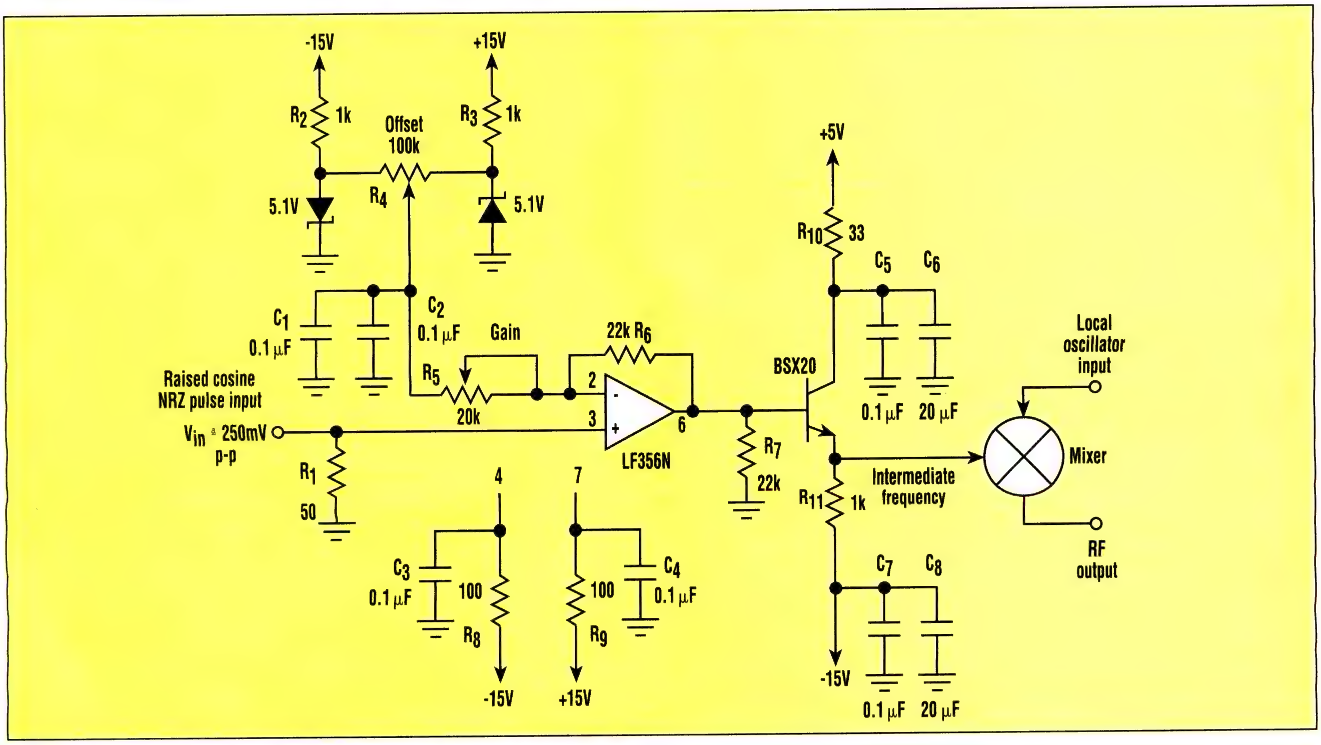
The circuit supplies typical bias currents of 5 to 10 mA for the Schottky diodes. Setup is most easily achieved with a clock input used as a data signal. This provides a static spectrum output signal that enables easy adjustment for maximum carrier and even-order sideband suppression. This condition coincides with near ideal constellation point locations.

The configuration was developed as a general-purpose solution, and is capable of interfacing to a wide class of mixer circuits.

Data rates are limited to around 512 kbits/s with the frequency-response specification of the LF356N op-amp.☐



2. MIXER output spectrum using a deficient driver (a) and the optimum driver (b) is given for an ideal unfiltered pseudorandom bit sequence input.

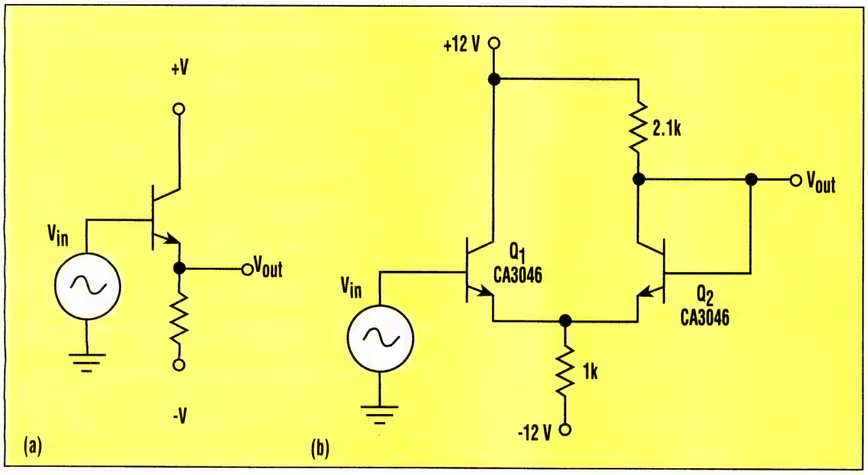


1. THIS OPTIMUM-SPECTRUM MIXER DRIVER supplies accurate power spectral translation by minimizing pulse degradation. Simultaneously, it enables optimum amplitude and dc offset levels to be applied.

CIRCLE 521

Low Voltage Offset Emitter Follower

MARC THOMPSON
19 Commonwealth Rd., Watertown, MA 02172.



AN EMITTER FOLLOWER is typically used when a unity-gain buffer is needed, but its voltage offset from input to output may be undesirable. A modified emitter follower (b) has matched transistors, Q1 and Q2, in the same package. Consequently, voltage offset and temperature drift will be reduced considerably.

In many cases, when a unity-gain buffer is needed, the ubiquitous emitter follower is employed *(see the figure, a)*, with its high input impedance and low output impedance. However, in a number of circumstances, the voltage offset from input to output (approximately 0.7 V, with a drift of –2.2 mV/°C) is undesirable. One technique used to reduce this offset involves cascading a pnp emitter follower with the npn follower. But matching npn and pnp parameters is a difficult task.

A simple alternative has matched transistors (Q1 and Q2) in the same IC package *(see the figure, b)*. Transistor Q2 is connected as a level-shifting diode and, to a first-order approximation, cancels the voltage shift in emitter-follower Q1. If Q1 and Q2 are matched with equal collector currents, and are in good thermal contact with one another, the voltage offset between input and output will be very small with little temperature drift. R_E and R_L are chosen so that at the operating point, the collector currents of Q1 and Q2 are equal.

The circuit is configured for a small input signal with 0-V dc value. For higher dc voltages, the resistors can be replaced by current sources. This ensures that the voltage offset remains approximately constant over a wider output-voltage range.☐

EDITORIAL CALL: WANTED—MORE IDEAS FOR DESIGN

We recently expanded the Ideas for Design section to include more items in each issue. To continue this expanded section, however, we will need a steady flow of ideas.

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Submissions to the Ideas for Design section should be about one typewritten page of text, with one or two circuit diagrams or block diagrams. They should represent the author's original work, be tested to prove they actually work, and not have been published previously. Please include telephone and fax numbers, if available.

Send your Ideas for Design to:

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611 Route 46 West
Hasbrouck Heights, N.J. 07604
Fax: 201-393-0204

CIRCLE 522

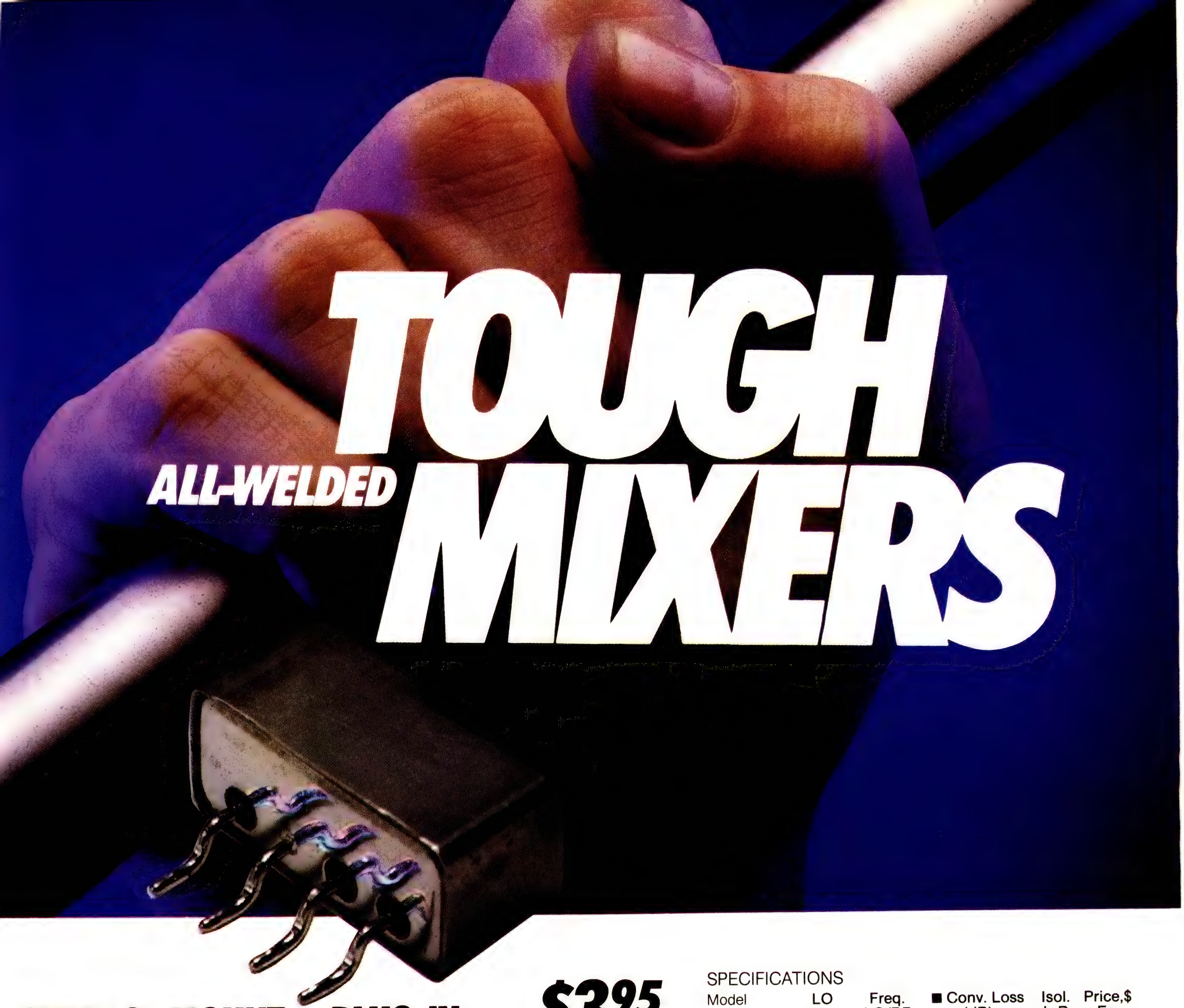
Fully Isolated RS-232 Port

MATT SMITH
Analog Devices, Raheen Industrial Estates, Limerick, Ireland.

This cost-effective, fully isolated, two-channel RS-232 interface provides isolation in excess of 2 kV, making it ideal for industrial communications that encounter large transients or noise *(see the figure)*. This circuit, when using a standard RS-232 interface, is also suitable for safely communicating with high-voltage equipment.

The circuit makes use of both magnetic and optical isolation techniques in which power is magnetically coupled across transformer T1 while data is optically coupled using two dual optocouplers. Only the transformer and the optocouplers will see the full 2 kV, so all other components comprise inexpensive low-voltage devices.

In the setup, a simple oscillator circuit formed using two inverters and an RC network generates a 150 kHz square wave. Two antiphase outputs are buffered and used to drive the bases of transistors Q1 and Q2. The transistors provide differential drive to transformer T1, which is a 1:1 center-tapped pulse transformer. The 150-kHz square wave on the primary is magnetically coupled across the transformer generating a ±10-V square wave on the secondary winding. This square wave is then recti-



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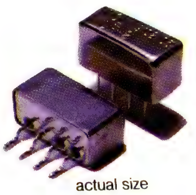

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SPECIFICATIONS

Model	LO Power (dBm)	Freq. LO/RF (MHz)	■ Conv. Loss (dB) $\overline{X}$	■ Conv. Loss (dB) δ	Isol. L-R (dB)	Price,$ Ea. 10 qty
TUF-3	7	0.15-400	4.98	0.34	46	5.95
TUF-3LH	10		4.8	0.37	51	7.95
TUF-3MH	13		5.0	0.33	46	8.95
TUF-3H	17		5.0	0.33	50	10.95
TUF-1	7	2-600	5.82	0.19	42	3.95
TUF-1LH	10		6.0	0.17	50	5.95
TUF-1MH	13		6.3	0.12	50	6.95
TUF-1H	17		5.9	0.18	50	8.95
TUF-2	7	50-1000	5.73	0.30	47	4.95
TUF-2LH	10		5.2	0.3	44	6.95
TUF-2MH	13		6.0	0.25	47	7.95
TUF-2H	17		6.2	0.22	47	9..95
TUF-5	7	20-1500	6.58	0.40	42	8.95
TUF-5LH	10		6.9	0.27	42	10.95
TUF-5MH	13		7.0	0.25	41	11.95
TUF-5H	17		7.5	0.17	50	13.95
TUF-860	7	860-1050	6.2	0.37	35	8.95
TUF-860LH	10		6.3	0.27	35	10.95
TUF-860MH	13		6.8	0.32	35	11.95
TUF-860H	17		6.8	0.31	38	13.95
TUF-11A	7	1400-1900	6.83	0.30	33	14.95
TUF-11ALH	10		7.0	0.20	36	16.95
TUF-11AMH	13		7.4	0.20	33	17.95
TUF-11AH	17		7.3	0.28	35	19.95

*To specify surface-mount models, add SM after P/N shown.

■ $\overline{X}$ = Average conversion loss at upper end of midband ($f_u/2$)

δ = Sigma or standard deviation

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F 145 REV.G

fied, generating an unstabilized +10 V dc supply.

Because the voltage is load-dependent, a standard 3-terminal voltage regulator is used to supply regulation to +5 V. Consequently, a stabilized and isolated +5-V power supply is derived.

The communications path is isolated using a pair of dual optocouplers. This facilitates two transmission and two receiving channels. TTL/CMOS logic signals on the grounded side are optically coupled across the isolation barrier, where they are then converted into RS-232 signal levels using an RS-232 driver.

These signal levels now are suitable for line driving. Handshaking signals coming from the opposite direction are converted into TTL/CMOS signals using an RS-232 receiver and then optically coupled in a similar fashion.

Ultimately, data rates in excess of 50 kbits/s are achievable using the components shown. If lower rates are acceptable, then less expensive (slower) optocouplers may be used.

Using the circuit as shown will provide a logic to RS-232 interface that can be easily designed into a system. If, however, isolating an existing RS-232 interface channel is desired, then this may be achieved by simply adding a second RS-232 transceiver at the logic interface. This would provide an RS-232 to RS-232 isolated interface that offers an equivalent (2 kV) level of isolation.

Furthermore, expanding the circuit to handle a larger number of communication channels is easily implemented by employing an appropriate number of optocouplers and RS-232 transceivers.☐

IFD WINNERS

IFD Winner for April 4, 1994

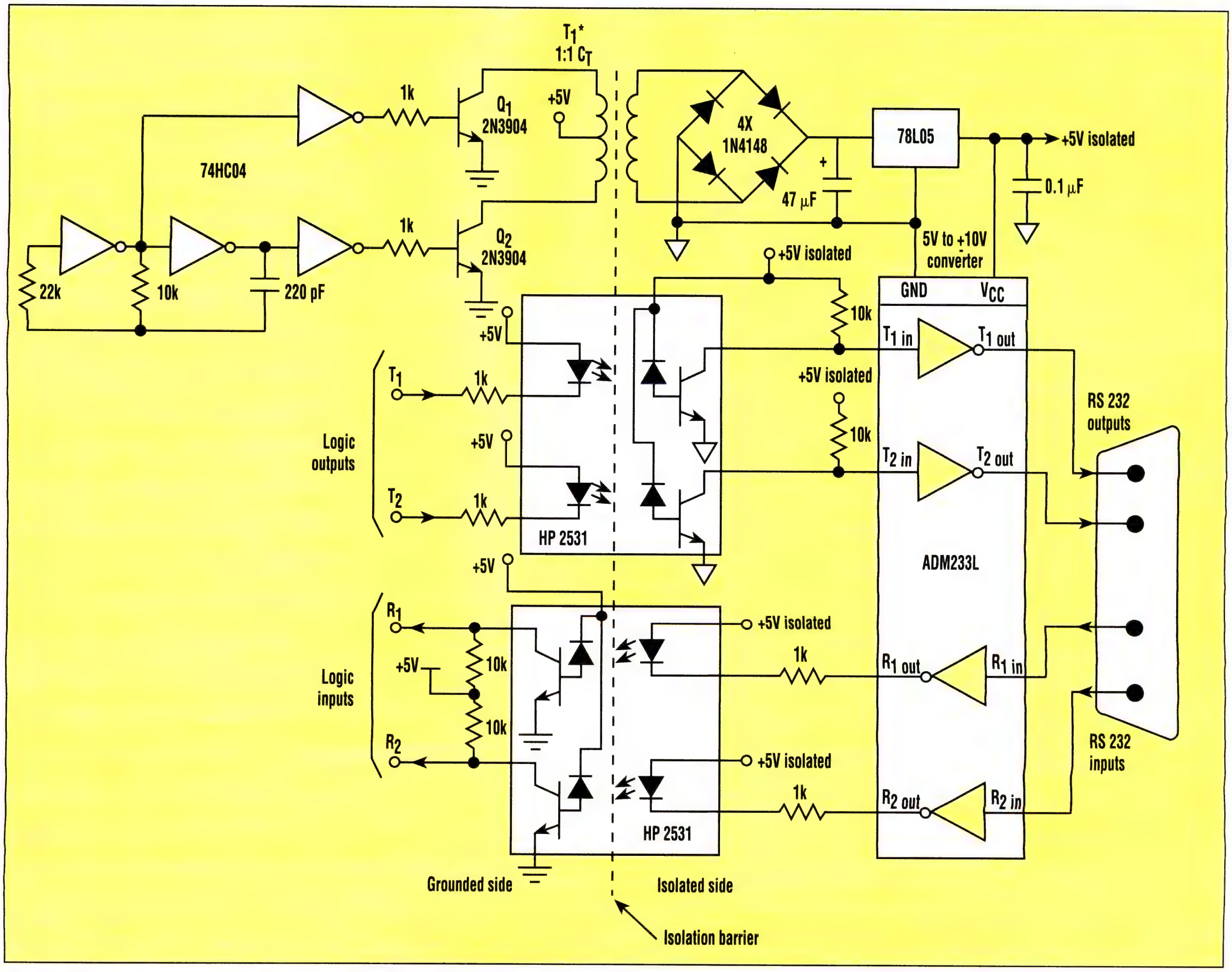
Alexander L. Belousov, 3806 Fords Lane, No. 201, Baltimore, MD 21215; (410) 764-1605. His idea: *"Simple Full-Wave Rectifier."*

IFD Winner for April 18, 1994

Don Bray, Horton Automatics, 4242 Baldwin Blvd., Corpus Christi, TX 78405; (512) 888-5591. His idea: *"Window Comparator Drives Bicolor LED."*

IFD Winner for May 2, 1994

George Altemose, Pall Instrumentation Technology, 95 Oser Ave., Hauppauge, NY 11788; (516) 273-0911, ext. 237, fax: (516) 951-2661. His idea: *"Build A Dimmer That Flickers."*



A TWO-CHANNEL RS-232 circuit that's fully isolated can be achieved with this setup. Isolation in excess of 2 kV is possible.

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UWR-5/4000-D12	9 - 36	5	4000	100	80%	C4	$76
UWR-12/1650-D12	9 - 36	12	1650	100	81%	C4	$76
UWR-15/1300-D12	9 - 36	15	1300	100	82%	C4	$76
UWR-5/500-D48	18 - 72	5	500	120	75%	C1	$45
UWR-12/250-D48	18 - 72	12	250	150	76%	C1	$45
UWR-15/200-D48	18 - 72	15	200	150	76%	C1	$45
UWR-3.3/1800-D48	18 - 72	3.3	1800	75	72%	C2	$66
UWR-5/1800-D48	18 - 72	5	1800	75	77%	C2	$66
UWR-12/750-D48	18 - 72	12	750	75	80%	C2	$66
UWR-15/600-D48	18 - 72	15	600	75	80%	C2	$66
UWR-3.3/4850-D48	18 - 72	3.3	4850	100	78%	C4	$76
UWR-5/4000-D48	18 - 72	5	4000	100	80%	C4	$76
UWR-12/1650-D48	18 - 72	12	1650	100	81%	C4	$76
UWR-15/1300-D48	18 - 72	15	1300	100	82%	C4	$76

Case Dimensions: C1 - 1.25" L x 0.80" W x 0.43" H C2 - 2.00" L x 1.00" W x 0.375" H
C4 - 2.00" L x 2.00" W x 0.45" H

Bipolar Models	V_{IN} Range (Volts)	V_{OUT} (Volts)	I_{OUT} (mA)	R/N (mV, p-p)	Efficiency (Min.)	Case	Price (100's)
BWR-5/1700-D12	9 - 36	±5	±1700	100	82%	C4	$76
BWR-12/830-D12	9 - 36	±12	± 830	100	81%	C4	$76
BWR-15/670-D12	9 - 36	±15	± 670	100	81%	C4	$76
BWR-5/250-D48	18 - 72	±5	± 250	120	73%	C1	$45
BWR-12/125-D48	18 - 72	±12	± 125	150	80%	C1	$45
BWR-15/100-D48	18 - 72	±15	± 100	150	80%	C1	$45
BWR-5/700-D48	18 - 72	±5	± 700	100	76%	C2	$66
BWR-12/415-D48	18 - 72	±12	± 415	75	79%	C2	$66
BWR-15/330-D48	18 - 72	±15	± 330	75	79%	C2	$66
BWR-5/1700-D48	18 - 72	±5	±1700	100	81%	C4	$76
BWR-12/830-D48	18 - 72	±12	± 830	85	81%	C4	$76
BWR-15/670-D48	18 - 72	±15	± 670	85	82%	C4	$76
Triple Models							
TWR-5/1200-12/250-D48	18 - 72	5/±12	1200/250	75/175	81%	C4	$76
TWR-5/1500-12/250-D48	18 - 72	5/±12	1500/250	75/175	79%	C4	$76
TWR-5/1800-12/200-D48	18 - 72	5/±12	1800/200	75/175	81%	C4	$76
TWR-5/1000-15/250-D48	18 - 72	5/±15	1000/250	75/175	79%	C4	$76
TWR-5/1500-15/250-D48	18 - 72	5/±15	1500/250	75/175	81%	C4	$76
TWR-5/1800-15/150-D48	18 - 72	5/±15	1800/150	75/175	80%	C4	$76

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CIRCLE 523

FIVE-COMPARATOR IC CONVERTS 3 V TO 5 V

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Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086;
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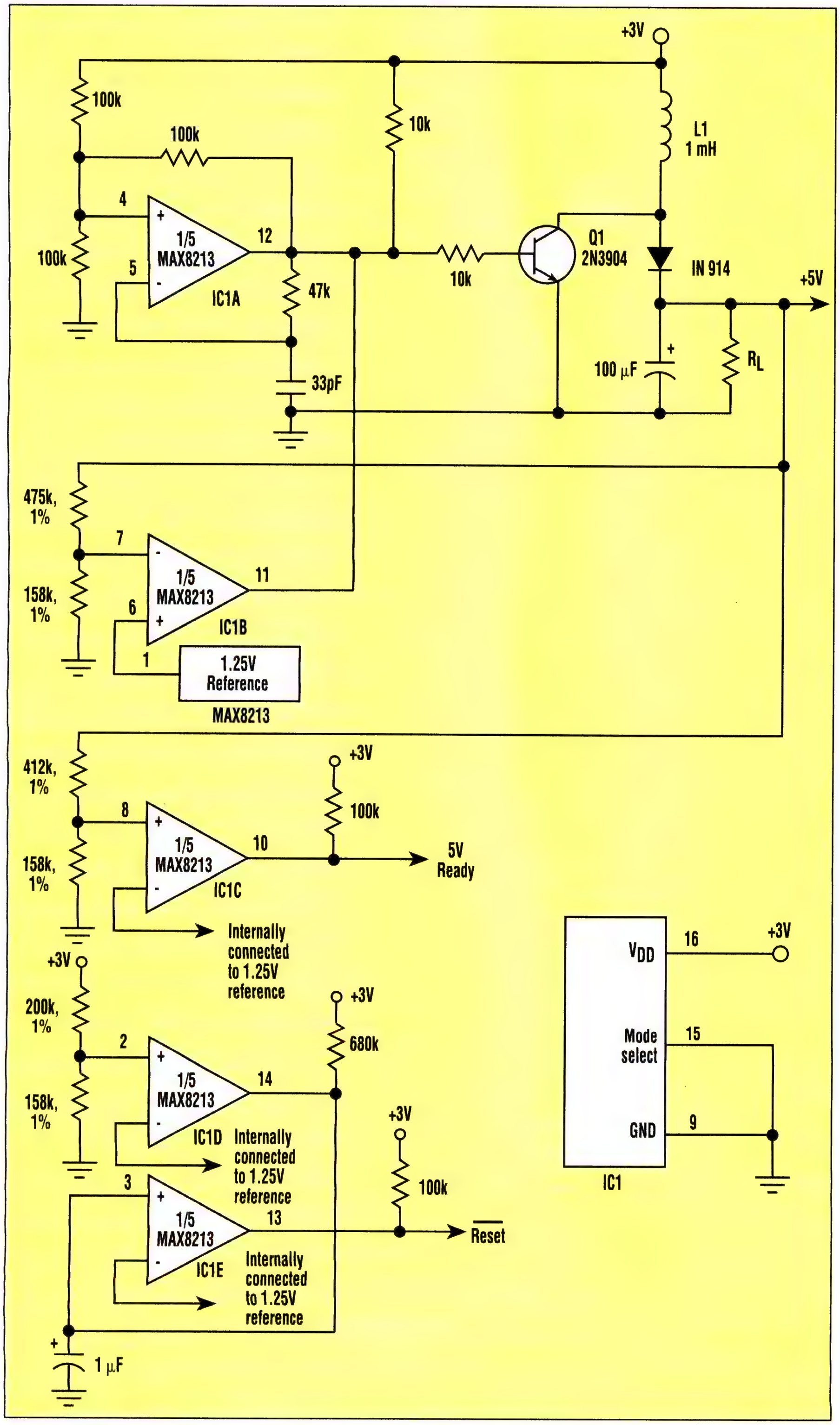

Although 3-V systems are becoming common, they often include at least a few 5-V components. A single five-comparator IC can produce the required 5 V (from 3 V) while also generating power-on reset signals for the system microprocessor *(see the figure)*.

In the circuit, comparator IC1A is configured as an oscillator whose square-wave output (with approximate 60% duty cycle) drives the base of Q1. Q1 drives a conventional dc-dc converter consisting of inductor L1, catch diode D2, and C_2. When V_{out} exceeds 5 V, comparator IC1B pulls the oscillator signal low (IC1's open-drain outputs may be tied together without doing harm). The net effect is regulation at 5 V.

IC1's minimum operating voltage is 2.7 V, and when the circuit is operated at that level, it can supply 2.8 mA at 5 V with 60% efficiency. L1 is an inexpensive 1-mH inductor with a series resistance of about 25 Ω.

For higher current and better efficiency, the inductor's resistance must be lowered by adding a more expensive inductor. Output ripple, which is almost entirely due to the hysteresis built into comparator IC1B, is about 50 mV.

Comparators IC1D and IC1E provide a reset signal for the microprocessor when the 3-V supply is too low (below 2.83 V). $\overline{\text{Reset}}$ goes low when the supply voltage falls below this threshold, and remains low for 200 ms after the supply voltage rises above the threshold.

For the positive-going supply voltage, hysteresis raises the threshold to approximately 2.87 V. The 200-ms interval assures time for a full reset of the microprocessor after power is restored. It also allows for time to recharge any capacitors associated with the circuit.

A related application for the five comparators of IC1 is to translate the logic signals generated by 3-V devices to the levels appropriate for 5-V devices.☐

THIS five-comparator circuit design and related components boost the 3-V supply to 5 V, issue a "5-V ready" signal, and also generate a microprocessor-reset signal.

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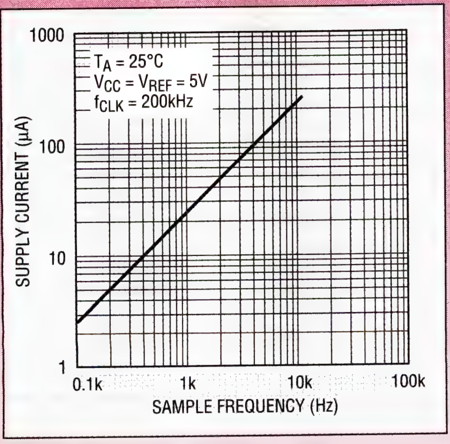

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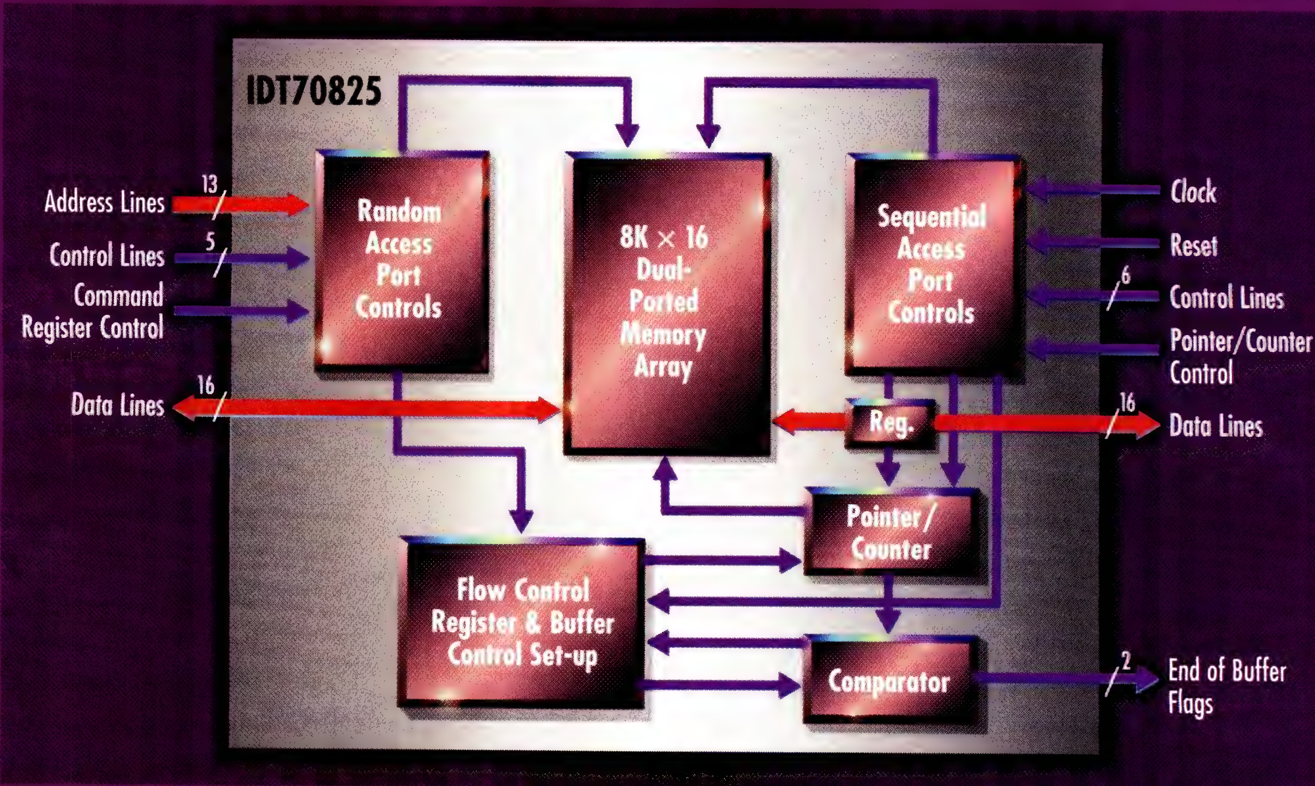

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PEASE PORRIDGE

WHAT'S ALL THIS V-F CONVERTER STUFF, ANYHOW? (PART I)

If you have already read Jim Williams' compilation, "Analog Circuit Design: Art, Science, and Personalities,"[1] *then you may look on this column as a summer rerun. However, several people, after reading my 1993 comments on Frequency-to-Voltage converters, asked my opinions on Voltage-to-Frequency Converters. I realized I had written all this down already, so here is a serialized version of the chapter I wrote in Jim's book—reprinted with the kind permission of Butterworth-Heinemann, Boston, Mass. Meanwhile, I'm going hiking.—RAP*

BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

Once upon a time, there were not any Voltage-to-Frequency Converters (VFCs) or any Voltage-Controlled Oscillators (VCOs). I couldn't tell you exactly when that was, but back in the 1950s and 1960s, very few people had ever heard about an oscillator whose frequency could be controlled by a voltage. In those days, when you wanted to change an oscillator's frequency, you usually changed a pot or a resistor or a capacitor, or maybe an inductor.

I checked up on this, because I spent a couple of hours searching in the old MIT *Radiation Lab Series*, published in 1949. There were no oscillators or multivibrators whose frequency could be controlled by a voltage—no VCOs, as far as you could learn by looking at the "Bible" of that time. (More comments to come on this in the next issue.)

It's true that FM radio transmitters used Frequency-Modulated oscillators, back as early as the 1930s, and these were modulated by voltages. But they only covered a relatively narrow frequency. When I refer to a VCO, I'm talking about oscillators whose frequency could be controlled over a range of 10:1 or 100:1 or 1000:1 or more. In general, this type of oscillator is expected to have a pulsed or square-wave output, *not* a sine wave.

Back in 1961, when I graduated from MIT and joined up with George A. Philbrick Researches (127-129 Clarendon Street, Boston 16, Mass.), I joined a company that made operational amplifiers, analog multipliers, integrators, and all sorts of Analog Computing Modules. And just about everything was made with vacuum tubes. There were Applications Notes and Applications Manuals that told you how to apply operational amplifiers (in those days we would never say, "op amp").

And there was the big old Palimpsest, a sort of collection of old stories on things you could do with operational amplifiers and analogue computing equipment. But, there were no digital voltmeters, and no voltage-to-frequency converters.

About 1963, I became aware of a high-performance operational amplifier—the 6043 project. This chopper-stabilized amplifier had been designed by Bruce Seddon, one of our senior engineers and VPs. The customer for this amplifier was Dymec, a subsidiary of Hewlett-Packard (if you turn *dy* upside down, does that look like *hp*?). And this amplifier was to be the front end of a Voltage-to-Frequency Converter instrument. The amplifiers were functioning pretty well, and they were meeting just about every specification. But they had a problem with undesired little offset shifts and jumps.

As the project went on, more and more engineers were looking over Bruce's shoulder, trying to help him solve this problem of the jumpy offset. Some people suspected that the amplifier stages might be rectifying out signals generated by ???, perhaps the transmitter of a local taxicab company? Other people suspected triboelectric effects, or electrochemical contamination.

I don't know if the cause of this drift or wobble was ever resolved—it was hard to resolve just a few dozen microvolts. But I have the impression that the amplifier project was not a success, and we never went into full production. If there was any circuitry of the actual VFC, that was never discussed at Philbrick—that was proprietary within Dymec, and our job was only to make an operational amplifier with low offset.

Of course, this amplifier had several vacuum tubes, and a chopper. The first amplifier tubes, 6CW4 nuvistors, ran with their 6-V heaters connected in series, so as to run on a 12-V dc bus and avoid the noises inherent in using 60 cps heaters. Then there were two more gain stages, dc-coupled. The chopper was an Airpax 172 or Bristol or similar, and there was a chopper amplifier based on a 12AX7. The whole circuit was similar to the Philbrick "USA-3" amplifier. It did, however, run on ±150 V instead of ±300 V. The late Dan McKenna, the senior technician who worked on the project, said he always suspected it was the fault of the heaters that were connected in series, because the data sheet on the 6CW4s said, "do not connect heaters in series."

But I realized later, connecting two heaters in series was surely OK; putting 10 or 20 tubes' heaters in series, as in a TV set, was the procedure that

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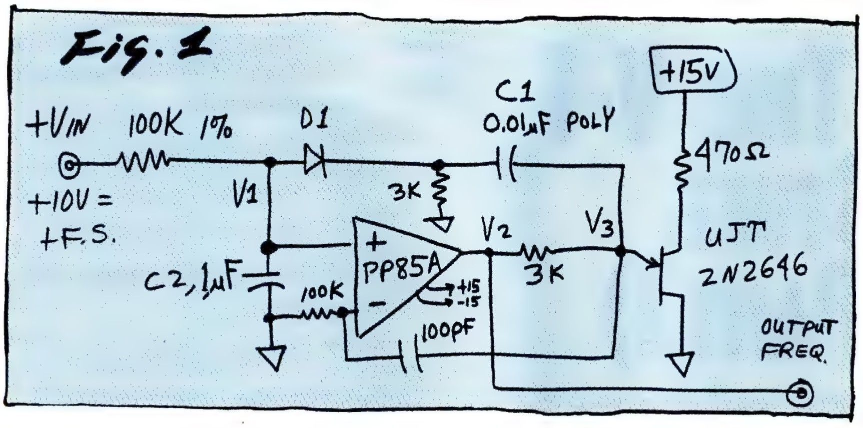


was prohibited. So, even though Dan grouched about it, this series stacking of 2 heaters was probably quite wise, not risky, because it would force the tubes to run at about the same amount of watts in each heater.

Anyhow, a design with vacuum tubes is Ancient History. Even then, although we were trying to design part of a V-to-F Converter, we didn't have a VFC in our lab. We didn't have a DVM—we had the old Fluke 805 Differential Voltmeters. Now, these meters have many elements of accuracy that good DVMs have these days, like good resolution and stability. But, they were big and heavy and slow. If you wanted to read 5.032 V, for example, you could do it, but it was a tedious deal.

You had to turn the first knob to 5, and then the next one to 0, and the next one to 3, and then turn up the Gain and look at the analog meter to see if the residue looked like a "2." That was how you learned the voltage was 5.032 V. If you've ever spent a few hours twisting the knobs of one of those old Fluke meters, you'll remember it with some nostalgia, but you must admit it was an awfully boring process.

When the first DVMs arrived from Hewlett-Packard and from Non-Linear Systems, they were slow and (in the case of the NLS) clunky and noisy, and they didn't have excellent accuracy or features compared to the old Fluke Differential Meters. But, they sure were faster and, of course, a lot easier to use.

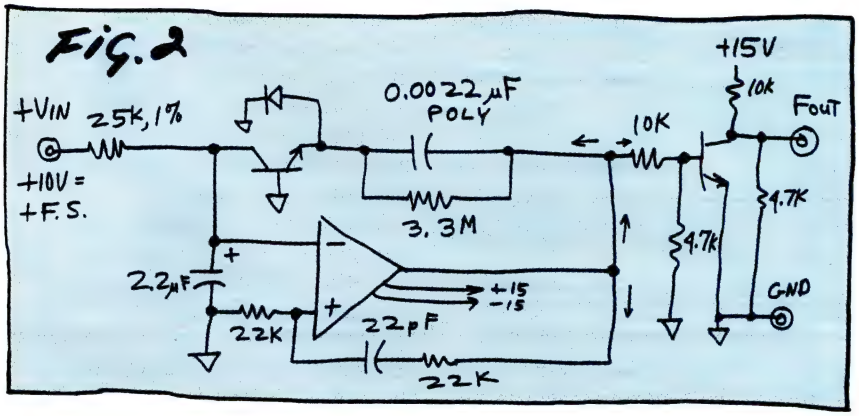
However, there was another way to do a DVM. You could buy a Voltage-to-Frequency converter from Dymec and feed its output frequency into an "Event Counter" (an EPUT meter—Events Per Unit Time—from Beckman Berkeley). Its neon-discharge display tubes would glow and tell you what the frequency was in terms of pulses per unit of time, and that was supposed to be linearly proportional to the input voltage.

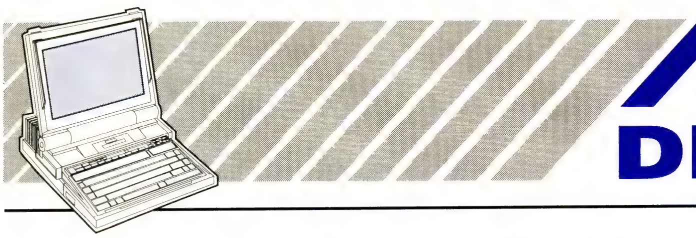
This new Dymec VFC had several solid-state circuits, and tricky pulse generators. To this day I don't know how those proprietary, secret pulse circuits were supposed to work. It had a pulse generator based on some special pulse transformers and blocking-oscillator circuits. The instrument had a pretty good tempco spec—but that's only because there was a little oven to hold all the transistorized circuits (which REALLY had a rotten tempco) at a constant temperature of +65°C. Consequently, when you turned it on, you had to wait at least half an hour before the accuracy would finally settle out to its ultimate value; in other words, waiting for the oven to settle its temperature. It could handle a full-scale voltage of ±1.0 V. It works pretty well. The VFC was claimed, originally, to have better than 0.02% of linearity. I measured one recently, and it had some nonlinear errors around 0.024%, which isn't bad. But, apparently, something had drifted slightly out of spec. It cost $1600, back when $1600 would buy you a Volkswagen. I still have one of the Dymec VFCs, Model DY-2211B, and the instruction book on it.

Now let's move up to about 1967. We engineers at Philbrick were working mostly on the design of solid-state operational amplifiers—amplifiers made of 6 or 8 or 10 discrete transistors and several resistors and capacitors in a compact potted module that was 1.125 in. by 1.125 in. by 0.5 in. The integrated-circuit operational amplifiers were arriving, but most of them were pretty crude in terms of performance and features.

One day, Bill Bernardi, one of the senior applications engineers, told me that a customer in Sweden had made a linear Voltage-to-Frequency Converter) using a PP85A (one of our standard operational amplifiers) and a UJT (UniJunction Transistor). And the nonlinearity was, he said, about 0.1%. When I heard this, I got kind of curious and skeptical, because everybody knows that UJTs are the crudest, dumbest, most imprecise oscillators you can find.

Just about every student learned that a UJT looks very cute because it can oscillate with a minimum amount of external parts—two resistors and one capacitor. BUT, it's an awfully junky circuit. You could gold-plate the sow's ear, and the UJT was still a junky circuit. Besides, I had recently





MAXIM DESIGN NEWS

Analog Design Insights from Maxim Integrated Products

No. 29

8-PIN BOOST CONVERTERS GIVE LONGEST BATTERY LIFE: 85% EFFICIENCY, 100µA I_Q, and 5µA SHUTDOWN

3.3V or 5V Step-Ups Use Small 11¢ Inductors and Have 1µA Shutdown

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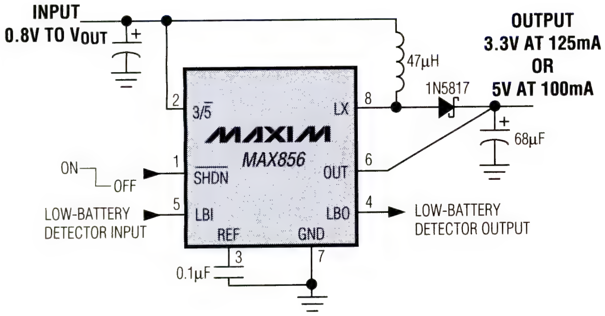
V_{OUT}: 3.3V, 5V, or Adj. (2.7 to 6V)



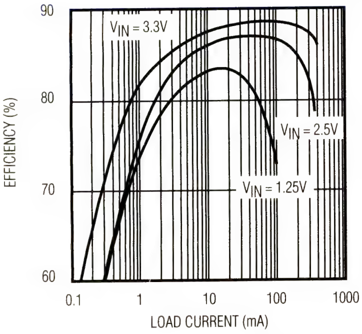
The 8-pin **MAX856/MAX857** (100mA output, 500mA switch current limit) and **MAX858/MAX859** (25mA output, 125mA limit) permit the use of small (2.6mm high), low-cost inductors to boost battery inputs from as low as 0.8V. Low 25µA quiescent supply current and 85% efficiency give long battery life. ($1.72, 1000 up)

READER SERVICE 243

2-Cell (1.8V) Step-Up Converters Maximize Battery Life at 3.3V or 5V Outputs

V_{IN}: 1.1V to 5.5V

V_{OUT}: 3.3V, 5V, or Adj. (2.5V to 5.5V)



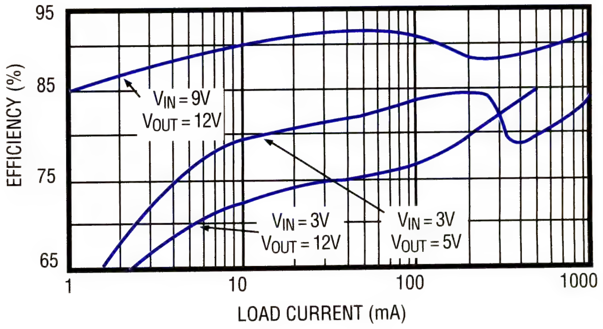
The 8-pin **MAX756** and **MAX757** have the world's best combination of high efficiency (>85% from 10mA to 300mA) and low quiescent supply current (60µA). Low 20µA shutdown and an input range down to 1.1V extend useful battery life. Guaranteed output is 300mA at 3.3V or 200mA at 5V. An LBI/LBO low-battery detector is built in. MAX756: preset 3.3V or 5V output. MAX757: adjustable 2.7V to 5.5V output. ($1.95, 1000 up)

READER SERVICE 245

3V-to-5V Step-Up Controller is >80% Efficient for 10mA to 1A Loads

V_{IN}: 1.8V to 16.5V

V_{OUT}: 5V, 12V, 15V, or Adj. (>3V)



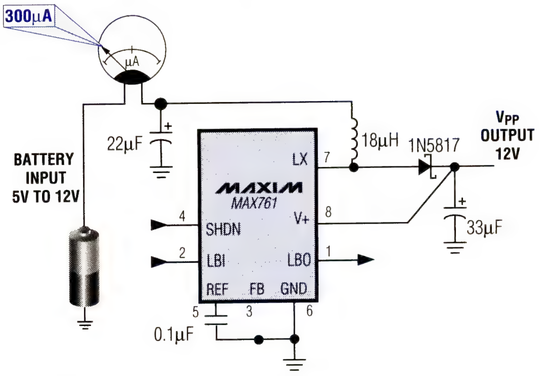
The **MAX770/MAX771/MAX772** drive external N-channel MOSFETs to boost inputs as low as 1.8V to preset 5V, 12V, 15V, or adjustable outputs limited only by the choice of external FET. Quiescent supply current is 110µA max. Shutdown is 5µA max. 300kHz switching frequency permits use of a 33µH inductor and 150µF capacitors. 8-pin DIP and SOIC packages. ($1.80, 1000 up)

READER SERVICE 244

Program 12V Flash Memories Using Only 300µA Quiescent Current

V_{IN}: 1.7V to 16.5V

V_{OUT}: 12V, 15V, or Adj. (2V to 16.5V)



The **MAX761** step-up converter delivers up to 120mA at 12V from inputs down to 3V. Shutdown supply current is 5µA, max. Efficiency is 88% from 5V_{IN} and 80% from 3V_{IN}. Fits in <0.3in^2. The **MAX762** has a 15V output. Both converters come in 8-pin DIPs and SOICs. An LBI/LBO low-battery detector is built in. ($2.23, 1000 up)

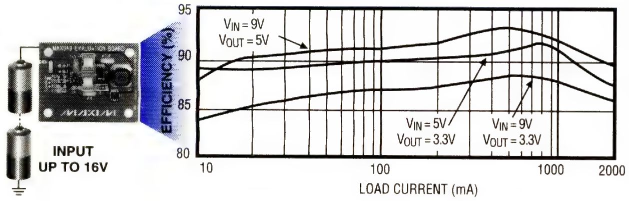
READER SERVICE 246

COMPACT STEP-DOWN AND INVERTING DC-DCs ARE 80%-95% EFFICIENT OVER 200:1 LOAD RANGE, DRAW <100µA I_Q

2A Step-Down Controller Uses Less Than 100µA I_Q

V_{IN}: 4V to 16.5V

V_{OUT}: 5V, 3.3V, 3V, or Adj. (1.5V to 16.5V)



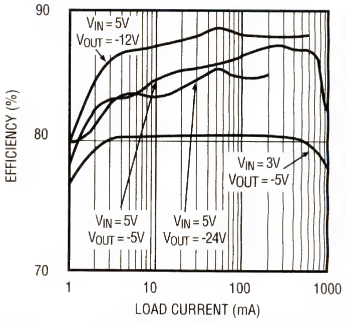
The compact 8-pin **MAX649/MAX651/MAX652** step-down controllers deliver 10mA to 2A with >90% efficiency. 5µA shutdown current reduces battery drain. Eliminates need for separate low-current back-up regulator. Drives external P-channel MOSFET. Uses 33µH inductor and 150µF capacitors. ($1.60, 1000 up)

READER SERVICE 247

High-Voltage DC-DC Inverter Biases -24V LCDs with 85% Efficiency

V_{IN}: 3V to 16.5V

V_{OUT}: -5V, -12V, -15V, or Adj. (< -1.5V)



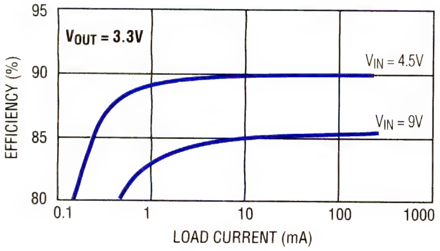
The **MAX774/MAX775/MAX776** DC-DC inverter controllers deliver 2mA to 500mA and come in 8-pin packages. Quiescent supply current is 100µA, max. Shutdown current is 5µA, max. They drive external P-channel MOSFETs, switch at up to 300kHz, and use 33µH inductors. Outputs are preset or adjustable using a potentiometer or resistors. *($2.20, 1000 up)*

READER SERVICE 248

200mA Step-Downs Draw <20µA Quiescent Current

V_{IN}: 4V to 11.5V

V_{OUT}: 5V, 3.3V, 3V, or Adj. (1.3V to 11.5V)



The **MAX639/MAX640/MAX653** are 88% efficient for 1mA to 200mA outputs—a 200:1 load range. Ideal for applications that mostly sleep and then deliver periodic high-power loads, such as detectors and back-up supplies. Logic-controlled shutdown. ($2.15, 1000 up)

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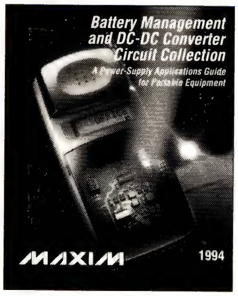
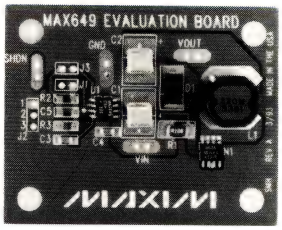
Free Samples, Evaluation Kits, and Literature

Free 58-Circuit DC-DC Converter Handbook





Preassembled surface-mount evaluation kits, and free samples and data sheets are available to speed your design cycles. A complete updated power supply design guide *(Design Guide #4, Rev. 6)* featuring the newest power supplies for your battery-powered and portable systems is now available. You can also order the **1994 Battery Management and DC-DC Converter Circuit Collection**, which contains 58 lab-proven power supply circuits for portable systems. To order, simply call Maxim or your local Maxim sales representative.

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PEASE PORRIDGE

built some Frequency-to-Voltage Converters, and it wasn't easy to get *them* to meet 0.1% linearity.

When I heard that a UJT was involved with a VFC of very good linearity, I was impressed, but also suspicious. So I looked into what they were doing. I didn't know anything about Voltage-toFrequency converters, but I was curious. I found that the PP85A was used as a comparator, and the UJT was mostly used to provide some "negative resistance," or positive feedback, to make a pulse whose amplitude or width aren't critical and thus didn't hurt the accuracy of the VFC. Ah, but how? How is it that a VFC which uses one simple comparator and a crude UJT pulser, and no other obvious precision components, provides a 0.1% linear VFC?

As near as I can recall and reconstruct, the circuit was basically that in Figure 1. The principle of operation is, that when the current from V_{in} causes the main integrating capacitor C2 to rise up to zero volts and the op amp starts to swing its output positive, the UJT is triggered. The UJT then puts out a crude pulse that kicks the minus input of the comparator. The output ALSO kicks a certain amount of charge through a charge-dispensing capacitor, C1, back to the integrating capacitor, to reset it. This amount of charge must be constant and invariant of anything, especially invariant of the repetition rate. If you can get that, you get excellent linearity. Apparently, the Swedish engineers had stumbled onto this crude but functional circuit.

Now that I understood the principles, I figured out that there was room for a good bit of improvement. I started fooling around with some breadboard circuits. I got the full-scale frequency up to 10 kHz (the Swedish circuit only worked well up to 1 kHz, which isn't nearly as useful), and got the nonlinearity down to 0.03%. And, I invented a scheme so that the operational amplifier's output could be capacitively coupled back to its + input, causing enough regeneration or positive feedback whereby the UJT was no longer needed. I used an Amelco 805BE integrated-circuit operational amplifier as the comparator.

Now, the whole circuit of Figure 2 fits into a 1.5-in. square package just 0.5-in. high—a small epoxy-potted module that was rather smaller than the PP85A amplifier and associated parts. We built up a prototype and tested it, and it worked pretty well. We potted it in our usual hard black epoxy, and shipped it to a customer in Connecticut—a customer of Larry Plante who was our Sales Engineer for that region.

Also, I sent in a Patent Application to our patent attorneys. I forget exactly who it was. Was it Curtis, Morris, and Safford in New York, or was it Schiller and Pandiscio in Waltham? No matter.

That must have been a busy year, because by the time I got off the other hot projects I had to work on for a number of high-priority customers, I realized I hadn't heard anything from this customer in Connecticut. I got in touch with Larry Plante.

All he knew was that the customer didn't like it. Worse yet, a whole year had elapsed since I had sent the part in interstate commerce, and the patent attorney had done nothing, so the patent application was now worthless.

I was quite cross, and I read the Riot Act at those attorneys. Then I set in at the workbench with a vengeance. And that led to the 4701 Voltage-to-Frequency Converter, which I'll tell you about in the next issue's Pease Porridge column.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

Address:
Mail Stop D2597A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

References:

1. *"Analog Circuit Design: Art, Science, and Personalities,"* edited by Jim Williams, 1991. 398 pages. Butterworth-Heinemann, Boston, Mass., (800) 366-2665. About $51. An excellent book; you should have your librarian order it.

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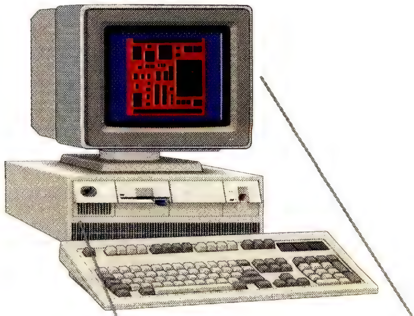

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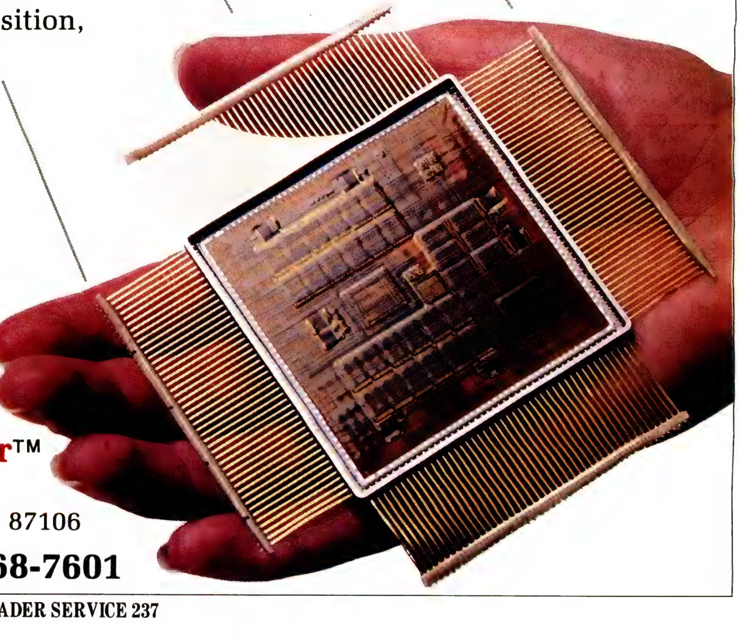


READER SERVICE 237

Communications Test Presents A Learning Curve

New terminology and evolving standards challenge designers.

BY JOHN NOVELLINO

Communications is one of the key technologies that will carry the electronics industry into the next century. Designers who haven't already begun verifying and characterizing communications systems' components stand a very good chance of getting involved in such projects in the near future.

For many of these engineers, the transition will require a significant learning experience. They will be working with a whole new lexicon, using terminology from standards that are new enough to still be evolving. Even the test equipment will be different. Much of it will be designed specifically for communications applications. Others will be traditional analog systems, like spectrum analyzers, brought into the digital arena.

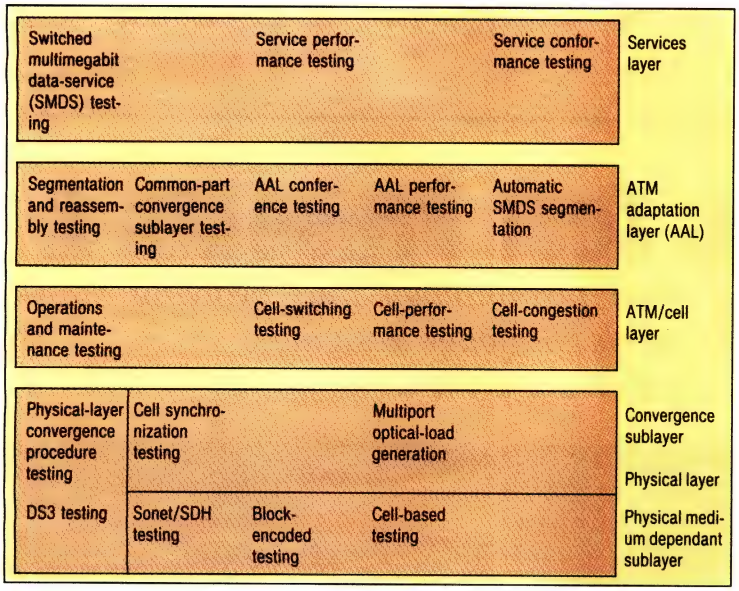
The hot topic at the moment—and the technology on which much work will be based—is asynchronous-transfer-mode (ATM) communications as it applies to the broadband Integrated Services Digital Network (B-ISDN). ATM is a fast packet-switched technology that telecommunications standards bodies have selected as the delivery vehicle for B-ISDN. It was first defined to run over the Synchronous Optical Network (Sonet) or the Synchronous Digital Hierarchy (SDH), but is becoming the technology of choice for many other existing physical interfaces.

ATM activity can be broken down into two broadly defined areas: the public networks, which are set up by common carriers to handle telecommunications traffic, and the private (or local-area) networks. The private networks will be ATM-based in the future, according to Gregan Crawford, a broadband test specialist at Hewlett-Packard's Telecom Test Div., Queensferry, Scotland.

1. A layered approach is usually recommended for testing broadband ISDN systems. Designers should start at the physical layer and work their way up the stack when it's appropriate for the system under test.

As far as testing goes, the initial emphasis has been on equipment for research and development. That's in accordance with the natural technology cycle that will eventually lead to greater emphasis on manufacturing test and then monitoring and maintenance equipment, says Crawford. "New areas are being explored all the time, and new interfaces are being defined by the ATM Forum, and we are reacting to that," he says. Crawford chairs the Forum's testing subworking group. He gauges ATM's increasing importance by the attendance at Forum's bimonthly meetings, which now numbers about 500.

The usual practice for designers working on ATM systems is to test their way up the protocol stack. They start at the bottom, the physical layer, which isn't ATM but a network interface like Sonet or DS3 *(see the figure)*. Here designers perform functional testing and transmission-convergence testing for the specific interface being used.


Switched multimegabit data-service (SMDS) testing
Service performance testing
Service conformance testing
Services layer
Segmentation and reassembly testing
Common-part convergence sublayer testing
AAL conference testing
AAL performance testing
Automatic SMDS segmentation
ATM adaptation layer (AAL)
Operations and maintenance testing
Cell-switching testing
Cell-performance testing
Cell-congestion testing
ATM/cell layer
Physical-layer convergence procedure testing
Cell synchronization testing
Multiport optical-load generation
Convergence sublayer
Physical layer
DS3 testing
Sonet/SDH testing
Block-encoded testing
Cell-based testing
Physical medium dependant sublayer

Testing then moves up to the ATM layer, which supplies a common transport mechanism for higher-layer services, and the ATM adaptation layer, which maps different types of service into the ATM cells. Finally, comes the services layer, where data is accepted from end applications and passed to the network for transmission.

When at the ATM layer, designers will want to check for cell loss, typically measured as a cell-loss ratio. This is analogous to measuring bit-error ratio at the physical layer. Instead of injecting a pseudorandom binary sequence and checking for lost bits, the tester will give sequence numbers to a string of cells and then look for missing numbers at the receive end.

Another needed measurement is cell delay, says Crawford. Designers must determine the delay caused in transitioning a specific piece of equipment as well as in the entire network. Delays can build up in a network if congestion occurs and data must be buffered in queues.

Getting into the details of the test procedures will require most engineers to learn a whole new set of terminology. Depending on their background, they may need to seek out seminars and classes for help, notes V. Prasanan, a product manager at Tektronix Inc. in Beaverton, Ore. The problem is that the standards documents contain nuances and references to standard practices that may not be meaningful to engineers who aren't in the telephony industry.

Besides the need for a specialized tester that targets the interfaces involved, some digital designers may have to acquire and learn to use a spectrum analyzer, an instrument traditionally employed by analog, especially RF, designers. "Even if you are not in the wireless area, you could need a spectrum analyzer because at speeds like 622 Mbits/s, harmonics are very important," says Prasanan. "They may have implications in your design that you may not be aware of."

In fact, most communications equipment will be subjected to EMI testing to comply with local, national, or international standards. That's a two-way street. The equipment must be tested for susceptibility to EMI to protect the integrity of transmissions. Strict standards also limit the amount of emitted electromagnetic radiation.

Some design teams will do their own ICs for their communications devices. Many, however, will rely on commercially available chip sets. Either way, designers must be thoroughly familiar with the standards. Even if the system is to use commercial chips, the designers shouldn't assume that those chips fully comply with the applicable standards, says Prasanan. And verifying compliance isn't a trivial task. "Do you understand the standards well enough to go and test the part to make sure it fits your design for your criteria? These are some of the things that you need to get into," he says.

Two testing problems that may not be familiar to designers of lower-speed digital systems, like computers, are jitter and pattern dependencies. In a computer, everything is normally timed off the same clock, but communications systems usually have multiple clocks. If those clocks aren't precisely synchronized in frequency, or phase, jitter results. Thus, jitter is similar to clock frequency modulation.

Designers must test their circuits for three jitter parameters. The first is how much jitter the system generates, with no input. The second is jitter tolerance—how much jitter can be applied with a test pattern running before bit errors occur. Finally, jitter transfer should be tested—the jitter that comes out after inputting a known amount of jitter.

Each interface standard defines its own jitter limitations, according to Jim McGrogan, a product marketing engineer at Anritsu-Wiltron Sales Co., Morgan Hill, Calif. These limits take the form of masks into which the system waveform must fit. Because of these different standards, and the general complexity of jitter measurements, McGrogan says designers need a one-button solution—an instrument that automatically compares the system signal to the appropriate mask and measures the needed parameters.

Jitter becomes more of a problem, both functionally and from a measurement standpoint, as system speeds rise. "In a data communications network where

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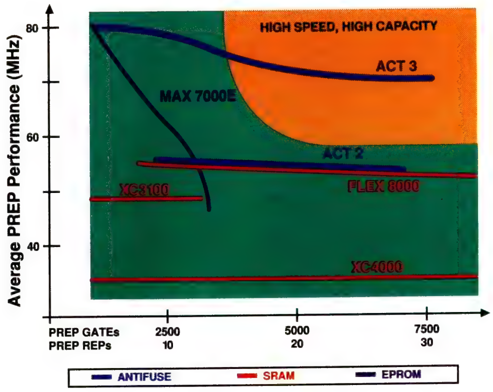

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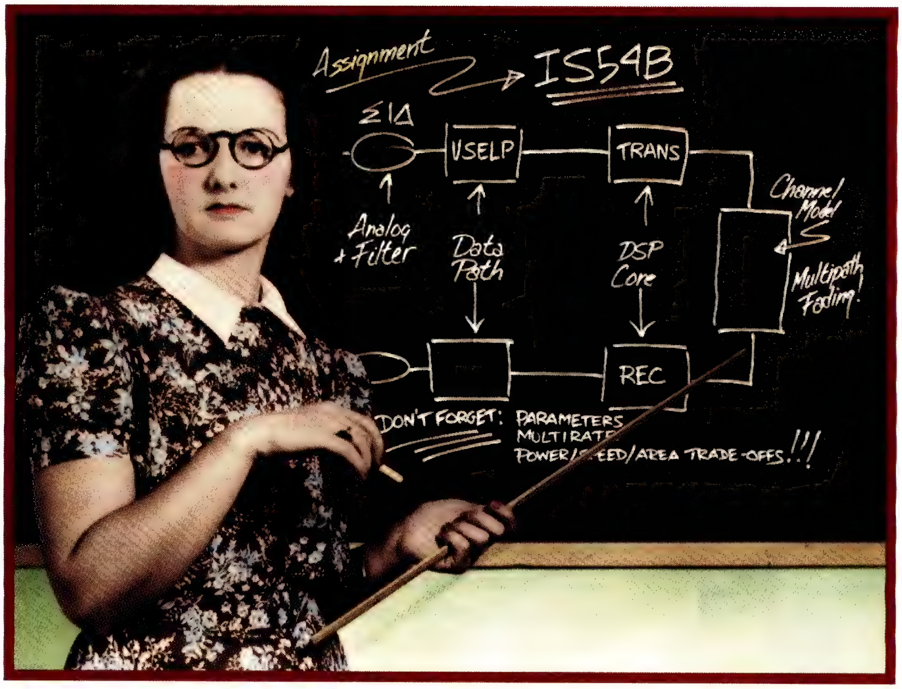

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you're running 2 Mbits/s, it's not very difficult to recover from phase jitter," says McGrogan. "But at the higher frequencies, for example 2.5 Gbits/s, jitter becomes a very critical issue. For that kind of application, you need a Sonet analyzer that does jitter testing."

Another test that must be considered concerns pattern dependencies. This is particularly true for optical systems, which use either ac coupling or devices such as laser diodes and detectors. The problem is that a change in the bit pattern may cause bit errors. Components should be evaluated for isolated patterns and framed patterns they may see in operation.

An isolated pattern involves a string of bits at one value, then a single bit at the other value, and a return to the original value. "So if you have all zeros, a one, and then go back to zeros again, a laser diode may not be quick enough to react to that type of pattern because of its coupling," says McGrogan. A bit-error test set can be used to check the components' reaction to isolated patterns, but a Sonet analyzer, which can create both framed and unframed patterns, should be used for a complete evaluation under real-world conditions, he says.

Because ATM networks will be able to handle different-bandwidth traffic from different customers and charge them accordingly, telecom-equipment buyers will want to specify precise performance levels. Designers, in turn, must be able to guarantee specific performance. This need also argues for real-world testing, and testing that stresses the equipment until it fails. This process entails not just system verification but characterization to determine precise limits, says Allan Campbell, a product manager in HP's IDACOM Telecom Div., Edmonton, Alberta, Canada. "Much in the way you use in-circuit emulators, what you need is in-network emulation, for want of a better description," he says. "What you want to do is have network traffic and load generation and simulation of real-world conditions as much as possible."

The testing process has been enlarged by the fact that the new network protocols are payload-independent, rather than payload-specific as in the past. As a result, designers will have to test their equipment not only for the type of protocol the customer may select, but also for the type of traffic: voice, video, or data. They must determine bandwidth limitations and throughput characteristics for each.

There are several factors potential users of communications test equipment should consider when looking for test sets. Some concerns are common to all test fields, but they take on greater importance in communications, in which test sets can be very expensive. For instance, as noted earlier, the standards are still evolving. Test equipment should be flexible enough to adapt to changes in the standards. Of course, designers should also consider what their next project, and the one after that, might be. They may be working at the lower layers now, but may have to do higher-layer testing in the future.

Also, with the importance of international sales these days, designers will want their new communications systems to be adaptable to standards worldwide. Although there are many similarities among the U.S., European, and Japanese standards, there are also many differences, some subtle, that must be accounted for. Test sets must handle these differences to let newly designed systems pass any required conformance tests.

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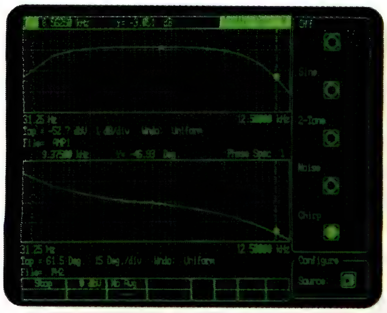

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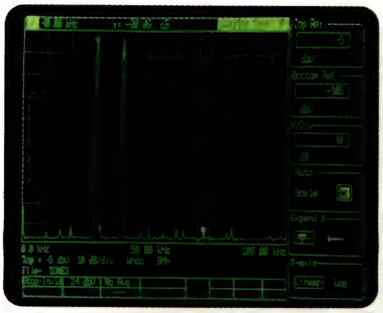

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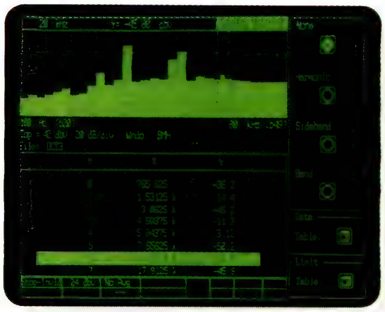

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Layered Approach Eases B-ISDN Testing

Design verification is easier when B-ISDN is stripped down to its individual layers.

BY WARD CAROLAN

Hewlett-Packard Telecom Operation, 31-41 Joseph St., Blackburn, Victoria 3130, Australia; 61 (3) 272-2957.

Asynchronous transfer mode (ATM) technology and the broadband Integrated Services Digital Network (B-ISDN) conjure up visions of utopia within the telecommunications community. The promise of one network technology for all services and of flexible bandwidth on demand tempts and tantalizes almost everyone in the telecommunications food chain. But many issues—technical, economic, and regulatory—are still unresolved.

A large engineering effort in hardware, software, and protocols is required to ensure equipment interoperability and performance. Hardware designs must continually develop as standards evolve and technology improves. An extremely important part of that process is the verification of equipment design through the means of rigorous testing.

During the design process, the various functional blocks of the equipment will be tested, typically with a logic analyzer. But this testing doesn't guarantee that an assembled module will meet the relevant standards and operate within specifications over permissible variations of power-supply levels and environmental conditions. For verification, the assembled equipment must be functionally tested at both its input and output ports.

The required verification testing can be very complex because of the numerous standards involved. Consequently, a layered testing approach has been adopted that takes advantage of the four-layer model that defines B-ISDN.

Designers must start by testing the physical layer and progress upwards. This approach makes sense as each layer can only be tested effectively if the layers below it operate correctly. If the physical layer has a fault, then none of the layers above it can be tested.

The B-ISDN standards still are evolving in a number of research and standards groups, such as the ATM Forum, Bellcore, ITU-TS, and others. These standards ultimately will provide the recommendations and specifications that form the basis of equipment conformance and interoperability, and thus determine the required testing. Therefore, before describing a layered testing approach to design verification, a detailed description of the B-ISDN model is necessary.

As noted, B-ISDN is defined by a four-layer model: the physical layer, ATM layer, ATM adaptation layer (AAL), and services layer. It's best to start the discussion at the second of these, the ATM layer, which is the core of the model.

The ATM layer supplies a common transport mechanism for different services—such as connectionless- and connection-oriented data, video, voice, and multimedia—over a range of different physical transmission interfaces. ATM communications employs a fast packet technology that combines the best features of circuit and packet switching. B-ISDN will transport, multiplex, and switch ATM cells to provide services between end users.

The basic transport unit, the ATM cell, has 53 bytes, consisting of a 5-byte header and a 48-byte payload *(Fig. 1)*. Two formats are used, one for the user-network interface (UNI) and another for the network-network interface (NNI).

The UNI format has a smaller range of virtual-path-identifier (VPI) values because it allocates the first four header bits to the flow-control function. The VPI and virtual-channel-identifier (VCI) bits form a label that identifies the switching path for each ATM cell. This label is overwritten by each ATM node according to its internal routing table, which translates physical input ports and VPI/VCI labels to corresponding output ports and labels.

The ATM layer uses certain ranges of VPI, VCI, and payload-type (PT) values for specific functions, like signalling and operations-and-maintenance (OAM) information. The three PT bits in octet four of the header indicate whether the payload is user data or F5 (VC) OAM information and whether the user data has experienced congestion in the network. The cell-loss-priority (CLP) bit is used to set priorities (0 is higher, 1 is lower) for the purpose of traffic-shaping and congestion prevention. The header-error-control (HEC) byte isn't the concern of the ATM layer but is inserted by the physical layer's transmission-convergence sublayer.

The physical layer applies to the transmission and reception of ATM cells across a physical medium (twisted pair, coaxial cable, or optical fiber) and consists of two sublayers, the physical medium-dependent sublayer and the transmission-convergence sublayer.

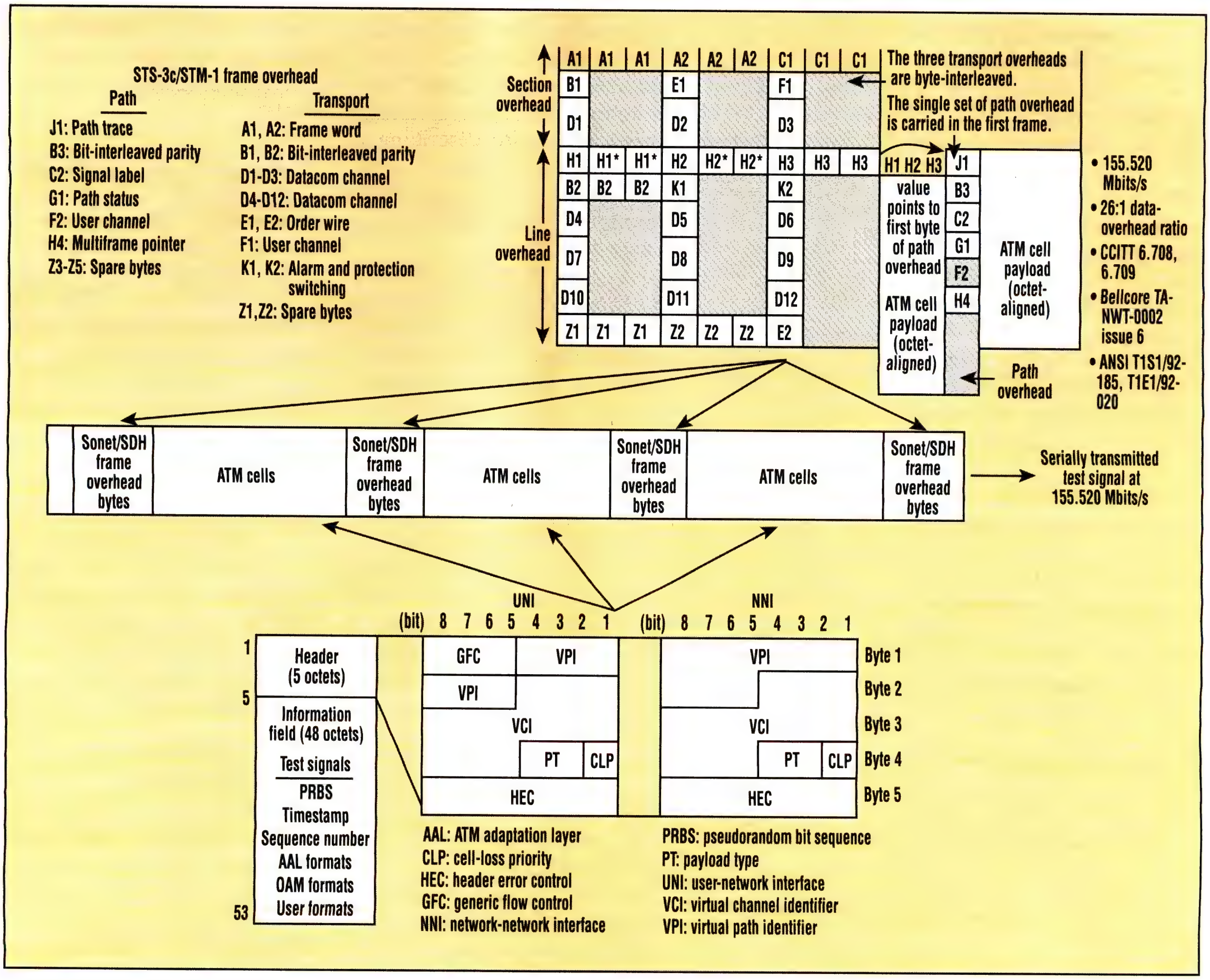
The physical medium-dependent sublayer transports the payload and overhead bits over the medium, as well as alarm and error-performance functions for the transmission link. The transmission-convergence sublayer maps ATM cells into the transmission-frame payload, adapts the cell rate received from the ATM layer to the available payload bandwidth by inserting idle cells, and provides header error correction using the HEC byte so that the receiver can delineate ATM cells and detect and correct or discard errored cells.

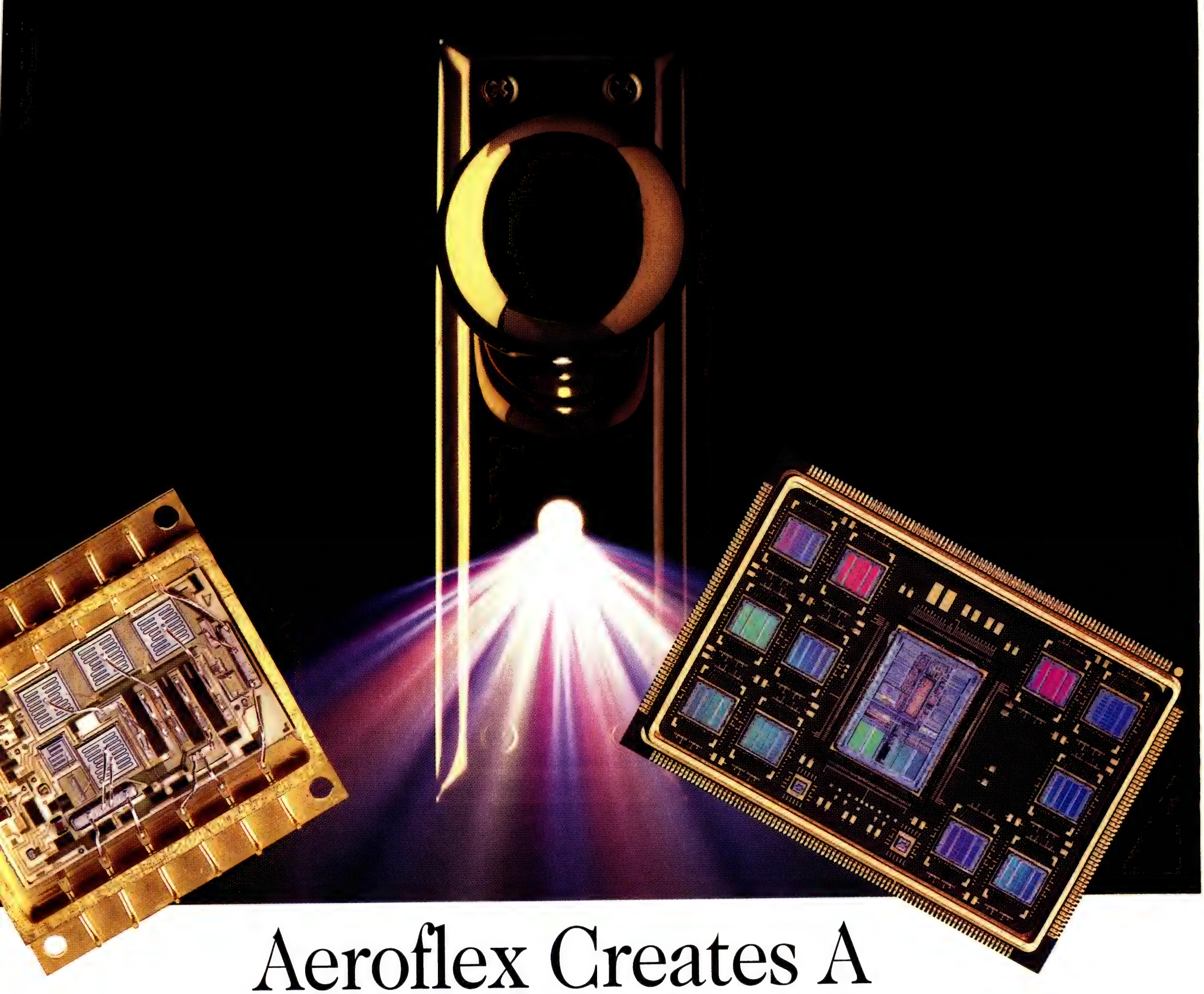
The AAL maps the variable-length frames of user data from the services layer to the fixed-size payload of the ATM layer. Different AALs are needed to provide the required end-to-end performance for different service types and classes. AAL1 is intended for constant-bit-rate services like circuit emulation, while AAL2 supports variable-bit-rate services such as video. AAL3/4 handles the mapping process for connectionless- and connection-oriented data services. AAL5, which is simpler and expected to be more efficient, may replace AAL3/4 in some applications and will also be employed for user-network and network-network signalling messages.

A significant feature of the current standards is the wide variety of interfaces specified for use with ATM technology. Initially, the synchronous optical network/synchronous digital hierarchy (Sonet/SDH) was envisioned as the transmission technology for the B-ISDN. That technology offers three data-transmission rates of 155 Mbits/s, 622 Mbits/s, and 2.488 Gbits/s. In addition, the payload can be concatenated to actually simplify the mapping of ATM cells.

But as companies race to develop ATM technology, the expense and limited availability of Sonet/SDH transmission facilities has required public carriers to use the existing plesiochronous-digital-hierarchy (PDH) transmission infrastructure for ATM communications. Specifications have been developed for 45-Mbit/s T3 and 1.5-Mbit/s T1 systems in the U.S.; 140-Mbit/s E4, 34-Mbit/s E3 and 2-Mbit/s E1 systems in Europe; and 6.3-Mbit/s J2 systems in Japan. The ITU-TS (formerly the

1. The basic transport unit for broadband ISDN is the ATM cell, which consists of 53 bytes. This includes a 5-byte header and a 48-byte payload.


STS-3c/STM-1 frame overhead
Path
Transport
J1: Path trace
B3: Bit-interleaved parity
C2: Signal label
G1: Path status
F2: User channel
H4: Multiframe pointer
Z3-Z5: Spare bytes
A1, A2: Frame word
B1, B2: Bit-interleaved parity
D1-D3: Datacom channel
D4-D12: Datacom channel
E1, E2: Order wire
F1: User channel
K1, K2: Alarm and protection switching
Z1,Z2: Spare bytes
Section overhead
Line overhead
A1 A1 A1 A2 A2 A2 C1 C1 C1
B1 E1 F1
D1 D2 D3
H1 H1* H1* H2 H2* H2* H3 H3 H3
B2 B2 B2 K1 K2
D4 D5 D6
D7 D8 D9
D10 D11 D12
Z1 Z1 Z1 Z2 Z2 Z2 E2
The three transport overheads are byte-interleaved.
The single set of path overhead is carried in the first frame.
H1 H2 H3 value points to first byte of path overhead
J1 B3 C2 G1 F2 H4
ATM cell payload (octet-aligned)
ATM cell payload (octet-aligned)
Path overhead
• 155.520 Mbits/s
• 26:1 data-overhead ratio
• CCITT 6.708, 6.709
• Bellcore TA-NWT-0002 issue 6
• ANSI T1S1/92-185, T1E1/92-020
Sonet/SDH frame overhead bytes
ATM cells
Sonet/SDH frame overhead bytes
ATM cells
Sonet/SDH frame overhead bytes
ATM cells
Sonet/SDH frame overhead bytes
Serially transmitted test signal at 155.520 Mbits/s
1
5
53
Header (5 octets)
Information field (48 octets)
Test signals
PRBS
Timestamp
Sequence number
AAL formats
OAM formats
User formats
UNI
(bit) 8 7 6 5 4 3 2 1
GFC
VPI
VPI
VCI
PT
CLP
HEC
NNI
(bit) 8 7 6 5 4 3 2 1
VPI
VCI
PT
CLP
HEC
Byte 1
Byte 2
Byte 3
Byte 4
Byte 5
AAL: ATM adaptation layer
CLP: cell-loss priority
HEC: header error control
GFC: generic flow control
NNI: network-network interface
PRBS: pseudorandom bit sequence
PT: payload type
UNI: user-network interface
VCI: virtual channel identifier
VPI: virtual path identifier



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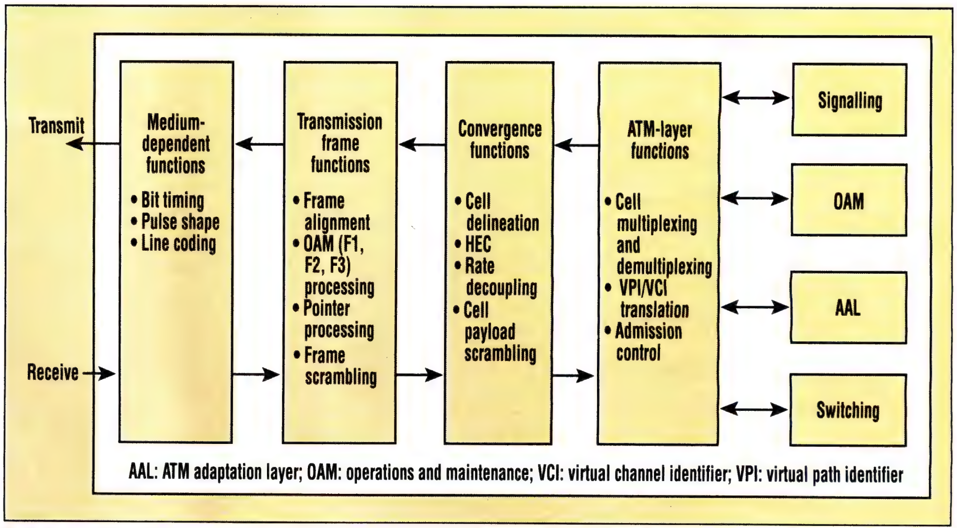
CCITT) G.804 specification is the cornerstone document for using these interfaces with ATM, although the ATM Forum also has done considerable work in this area.

Higher-order PDH systems, however, generally aren't found in the local-area environment where shielded and unshielded twisted pair (STP, UTP3, and UTP5) and multimode optical fiber predominate. These existing technologies must be used if ATM is to be cost-effective. The ATM Forum is addressing this need and has already specified interfaces for use on multimode optical fiber (100 Mbits/s and 155 Mbits/s block-encoded) and STP (155 Mbits/s block-encoded). The ATM Forum also is considering Sonet interfaces at data rates of 52 and 155 Mbits/s over UTP and STP using a carrierless amplitude-modulation scheme.

ATM equipment generally falls into two categories: network equipment and end-user equipment. Network equipment, such as an ATM switch, transmits and switches ATM cells and generally doesn't interface directly to the service layer. Consequently, it won't perform AAL functions, except for AAL5, which is needed by the signalling function. End-user equipment, such as a workstation or server with ATM interfaces, must map services into the ATM layer so that it implements AAL functions.

As noted, design verification should take a layered approach, based on the B-ISDN model. The approach described here uses a block diagram of the model in which the layers are depicted as functional blocks of ATM equipment. The block diagram is generic in that it includes the functions that would be found in both network and end-user equipment *(Fig. 2)*. Designers can test various aspects of their equipment by simulating and monitoring a number of conditions in the frame overhead, cell header, and cell payload. For this discussion, the test-signal format uses the 155-Mbit/s Sonet/SDH physical layer *(Fig. 1, again)*.


Transmit
Receive
Medium-dependent functions
• Bit timing
• Pulse shape
• Line coding
Transmission frame functions
• Frame alignment
• OAM (F1, F2, F3) processing
• Pointer processing
• Frame scrambling
Convergence functions
• Cell delineation
• HEC
• Rate decoupling
• Cell payload scrambling
ATM-layer functions
• Cell multiplexing and demultiplexing
• VPI/VCI translation
• Admission control
Signalling
OAM
AAL
Switching
AAL: ATM adaptation layer; OAM: operations and maintenance; VCI: virtual channel identifier; VPI: virtual path identifier

2. This functional block diagram, which is based on the multi-layered B-ISDN model, will help designers break down the verification task into more easily handled segments.

The physical layer performs three distinct groups of functions: medium-dependent, transmission frame, and convergence. Technically, the latter two functions form the transmission-convergence sublayer, but they differ from a testing perspective.

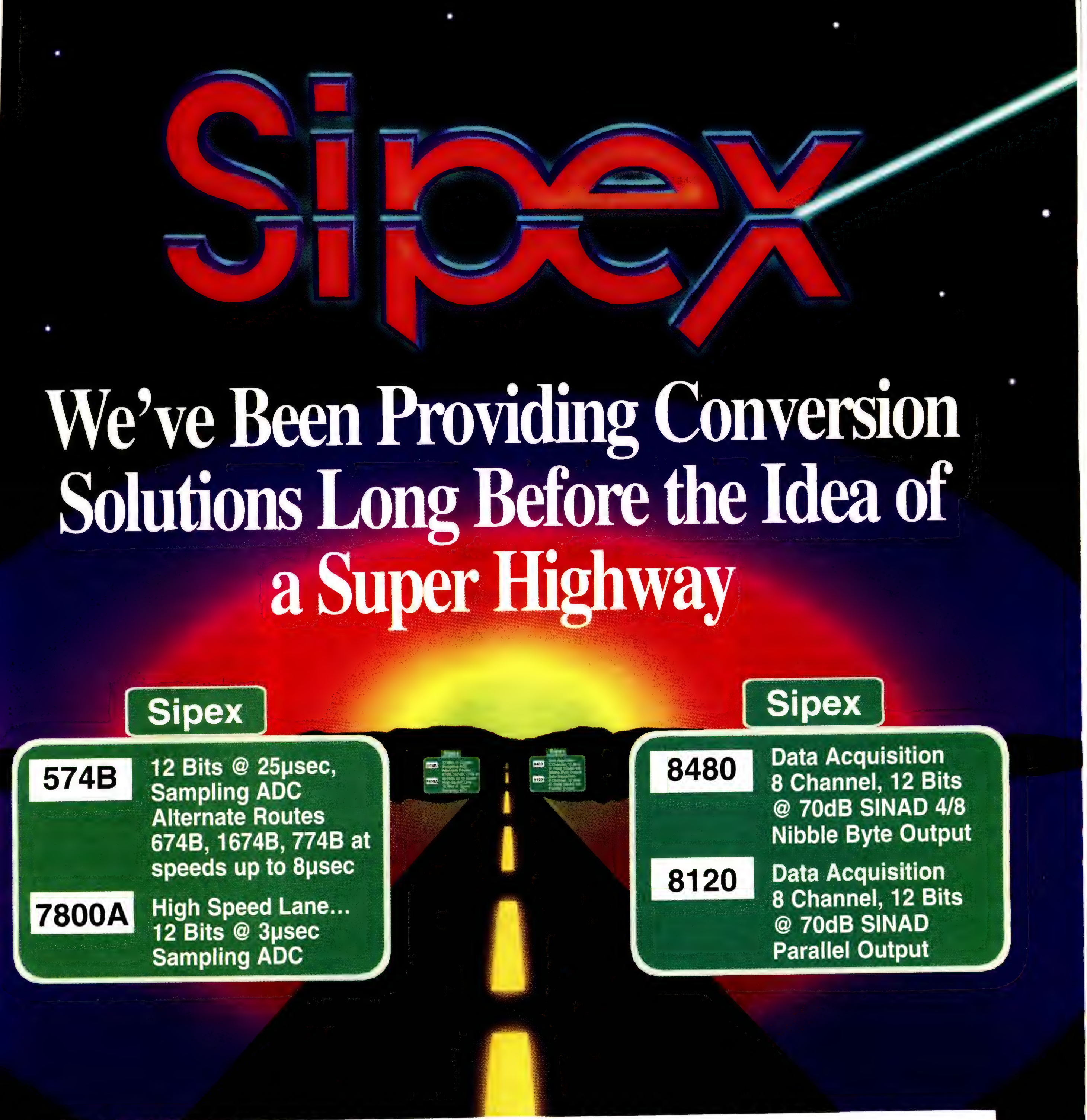
Medium-dependent functions involve transmitting and receiving a bit stream over the transmission medium. To verify the correct operation of these functions, designers must measure the characteristics of impedance, return loss, output pulse shape, receiver sensitivity, clock stability and retiming, and jitter. If an optical medium is used, wavelength, optical output power, and pulse dispersion also must be measured. These measurements aren't specific to B-ISDN equipment, but are common to all transmission interfaces.

The transmission-frame functions generate and recover the transmission frame and process the frame overhead. As might be expected, the amount of testing needed is proportional to the functions supplied by the transmission frame.

Sonet/SDH frames, for instance, carry lots of overhead to manage functions like regenerator sections, line sections, and the end-to-end transmission path. At the other end of the spectrum, the 100-Mbit/s block-encoded interface recommended by the ATM Forum has little or no overhead functions. In between, the PDH interfaces' frame overhead includes a frame-alignment signal, some form of frame error checking (usually based on a cyclic-redundancy-check code), and alarm information.

The Sonet/SDH frame for STS-3c/STM-1 has a line rate of 155 Mbits/s and consists of section, line, and path overhead parts, as well as a concatenated payload that contains the ATM cells *(Fig. 1, again)*. To achieve higher line rates, multiple STS-3c/STM-1 frames are synchronously multiplexed using byte interleaving to form similar frame structures at 622 Mbits/s and 2.488 Gbits/s. Because the payloads are concatenated, the additional overhead bytes are redundant at these higher rates. Thus, ATM applications testing is similar at all three rates. The functions that must be tested in a Sonet/SDH frame are frame alignment, alarm operation, error-performance monitoring, and pointer processing.

The A1 and A2 bytes (binary value 11110110 and 00101000) form the frame alignment pattern. To verify that these bytes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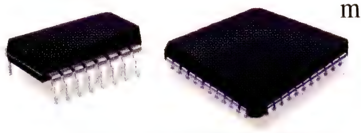

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are correctly transmitted, the measuring instrument must count any errors received in these bytes.

Verifying receiver operation becomes a little more complex. The tester must implement the loss and recovery of a frame algorithm as described in the ITU-TS G.783 document and the Bellcore TA-YSY-000253 document. Two states, out of frame (OOF) and loss of frame (LOF), are specified. OOF is declared when four or more consecutive errored framing patterns are received. If OOF persists for 3 ms (24 frames), LOF is declared.

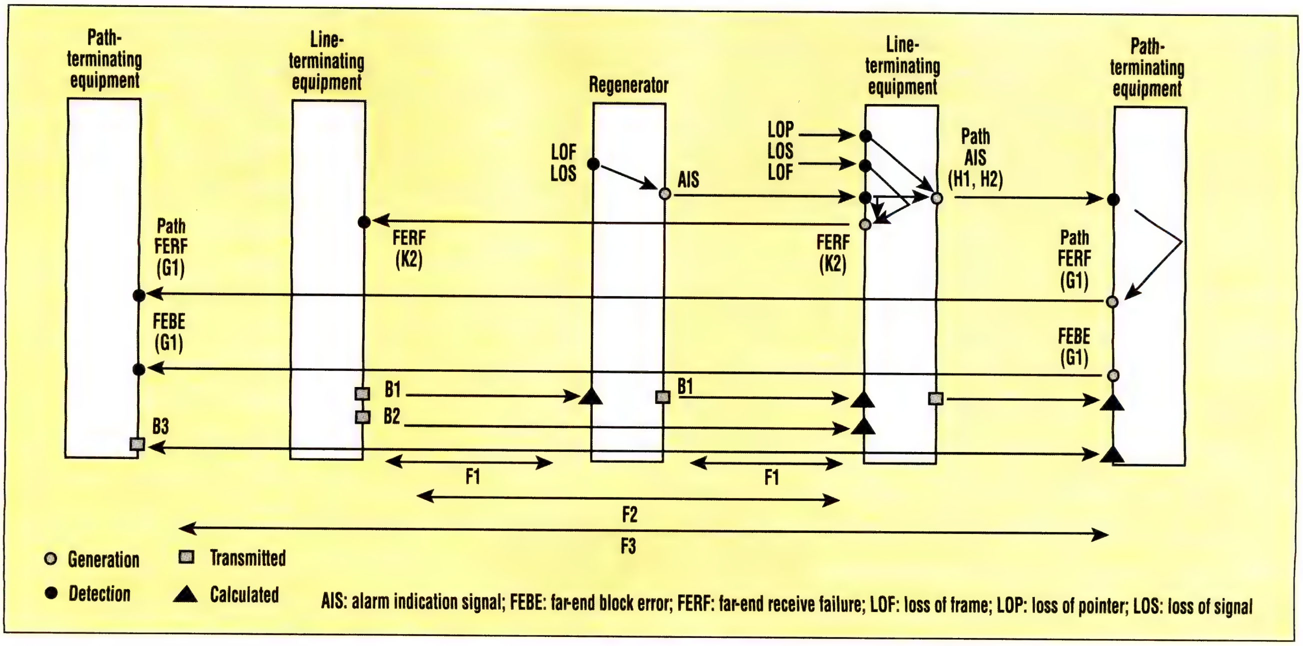
Recovery from OOF and LOF requires a valid framing pattern to be detected for a duration of 250 μs (two frames) and 1 ms (eight frames), respectively. Testing under this algorithm requires a Sonet/SDH test signal containing consecutive errored framewords that are at, above, and below the specified thresholds. This can be done with a stressing algorithm that allows a burst of "p" consecutive errored framewords, followed by a repeating cycle of "n" valid framewords and "m" errored framewords. Being able to set p, n, and m between 0 and 64 (each frame corresponds to a time of 125 μs) allows the frame-alignment algorithm to be fully tested.

The remaining overhead performs several functions at the section (between regenerators), line (between line-terminating equipment), and path (between switch nodes) levels. These are defined as the F1, F2, and F3 OAM functions by the ITU-TS I.610 document *(Fig. 3)*. The alarm and error-monitoring functions at each level are contained in the K1, K2, G1, B1, B2, B3, and Z2 bytes. The remaining bytes provide data and voice channels for maintenance purposes and carry pointer information needed for the synchronization process.

Alarm operation involves detecting various conditions and taking appropriate actions. The matrix of conditions and actions at the F1, F2, and F3 levels is extensive, but they follow common principles. If an invalid signal is received, an alarm indication signal (AIS) is sent downstream, and a far-end receive failure (FERF) is sent upstream. The test instrument must be able to generate and receive the appropriate overhead bytes to do such testing.

Error monitoring uses the bit-interleaved-parity (BIP) technique with even parity. The B1, B2, and B3 bytes contain the parity value calculated over the previous frame. Correct values can be verified if the instrument receiver recalculates the parity values for a given frame and compares them with the values received in the next frame, counting any errors that occur. Generating errored B1, B2, and B3 bytes will ensure that the equipment receiver can correctly perform BIP processing. The equipment should also send a far-end block-error (FEBE) indication in response to an errored B2 or B3 byte. Line-FEBE indication is sent in the Z2 byte of the transport overhead, and Path-FEBE indication in the G1 byte of the path overhead.

To maintain synchronization between the path payload and the Sonet/SDH line clock, the signal uses pointer processing. Pointer values contained in the H1, H2, and H3 bytes indicate the position of the first payload byte relative to the pointer position in the transport overhead. The path overhead contains an H4 pointer, but it's not used for ATM because the HEC delineation process identifies the ATM cell positions in the payload. To test the equipment transmitter, the rate and phase of the line and



AIS: alarm indication signal; FEBE: far-end block error; FERF: far-end receive failure; LOF: loss of frame; LOP: loss of pointer; LOS: loss of signal

3. The F1, F2, and F3 operations and maintenance functions include alarm and error-monitoring capabilities.

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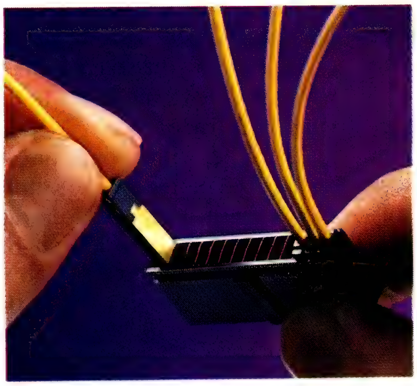

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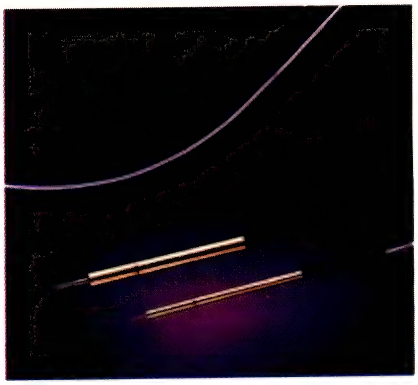

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payload clocks can be individually adjusted and the resulting pointer operations measured. A Sonet/SDH test signal that simulates pointer operations can be used to exercise the equipment receiver.

To complete testing of the transmission-convergence sublayer, two important functions must be checked—cell delineation and rate adaption. These involve HEC procedures and idle-cell insertion and extraction. HEC procedures are checked by ensuring that the equipment transmitter is correctly generating the HEC byte and that the receiver is correctly recovering it and performing error detection and correction. The HEC byte is calculated over the first four header bytes according to an algorithm specified in the ITU-TS I.432 document.

To minimize the possibility of the header data being duplicated in the cell payload, the payload is scrambled (using the self-synchronizing scrambler polynomial X43+1).

Designers can verify the transmitter's operation using an instrument receiver that accurately implements the HEC synchronization algorithm and detects any cells with invalid HEC bytes. The transmitter must send an ATM cell stream at full bandwidth, with a variety of VPI and VCI values to ensure some variance in the HEC calculation. The instrument receiver measures HEC error count and HEC error ratio. Ideally, no errors should be detected. The HEC mechanism allows for the correction of single-bit errors and detection of multiple-bit errors. If HEC errors are detected, measuring correctable and non-correctable errors may offer useful troubleshooting information.

The scrambling process can be tested by sending a pseudo-random bit sequence (PRBS) in the cell payload of the test signal and measuring the payload bit-error ratio. This measurement must be performed with and without scrambling to be sure any errors detected are due to the scrambling process.

On the receive side, the equipment examines the incoming bit stream, bit by bit, until it recognizes a valid HEC byte in any five-byte sequence. In this "presync" state, the receiver then checks every 53rd byte for a valid HEC value. If it detects seven consecutive valid HEC bytes, the receiver goes into the sync state. The receiver continues to monitor the HEC bytes, and if six consecutive invalid bytes are detected, synchronization is lost. The receiver then moves into the hunt state and restarts the procedure of bit-by-bit examination.

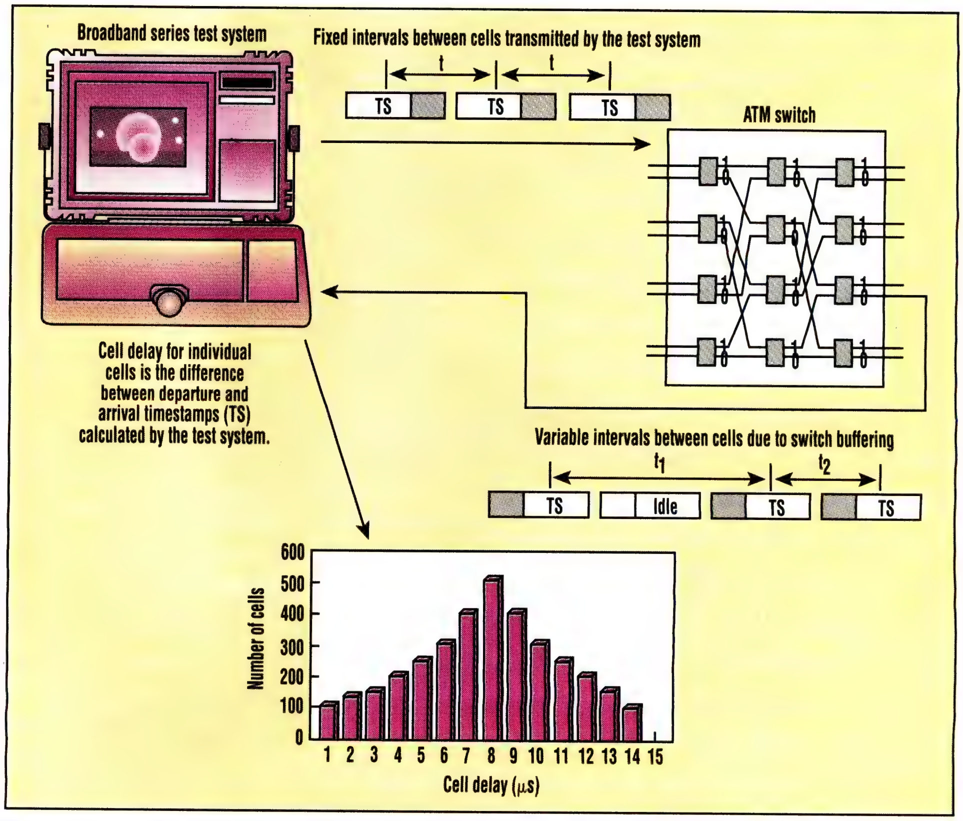
To test this delineation process, the instrument transmitter must supply a full-bandwidth ATM cell stream with errored HEC bytes that simulate conditions below, at, and above the thresholds of the presync, sync, and hunt states. The same p, n, and m stressing approach used for testing Sonet/SDH frame alignment can be used for this purpose. Errors can be introduced by applying an error mask to toggle one or more bits of the valid HEC byte.

The other important convergence function designers must test is the insertion and extraction of idle cells to match the ATM layer's cell bandwidth to the maximum supported by the physical interface. This testing can be done by generating an ATM-layer cell stream with a variable bandwidth, and filtering and measuring the idle and ATM-layer bandwidths in the receiver.

Designers can now move to the ATM layer, whose basic function is to route cells and manage congestion. The routing function is associated with the multiplex and demultiplex processes, and with the switch fabric in the case of an ATM switch.

On the receive side, an ATM interface demultiplexes cells containing user data, OAM, and signalling information, and then passes them to the appropriate higher-layer processes via a ser-

4. Delay measurements are made by adding timestamps to the ATM cells. The test instrument usually presents the results in a histogram form.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t
TS
TS
TS
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Variable intervals between cells due to switch buffering
t_1
t_2
TS
Idle
TS
TS
Number of cells
600
500
400
300
200
100
0
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Cell delay (μs)

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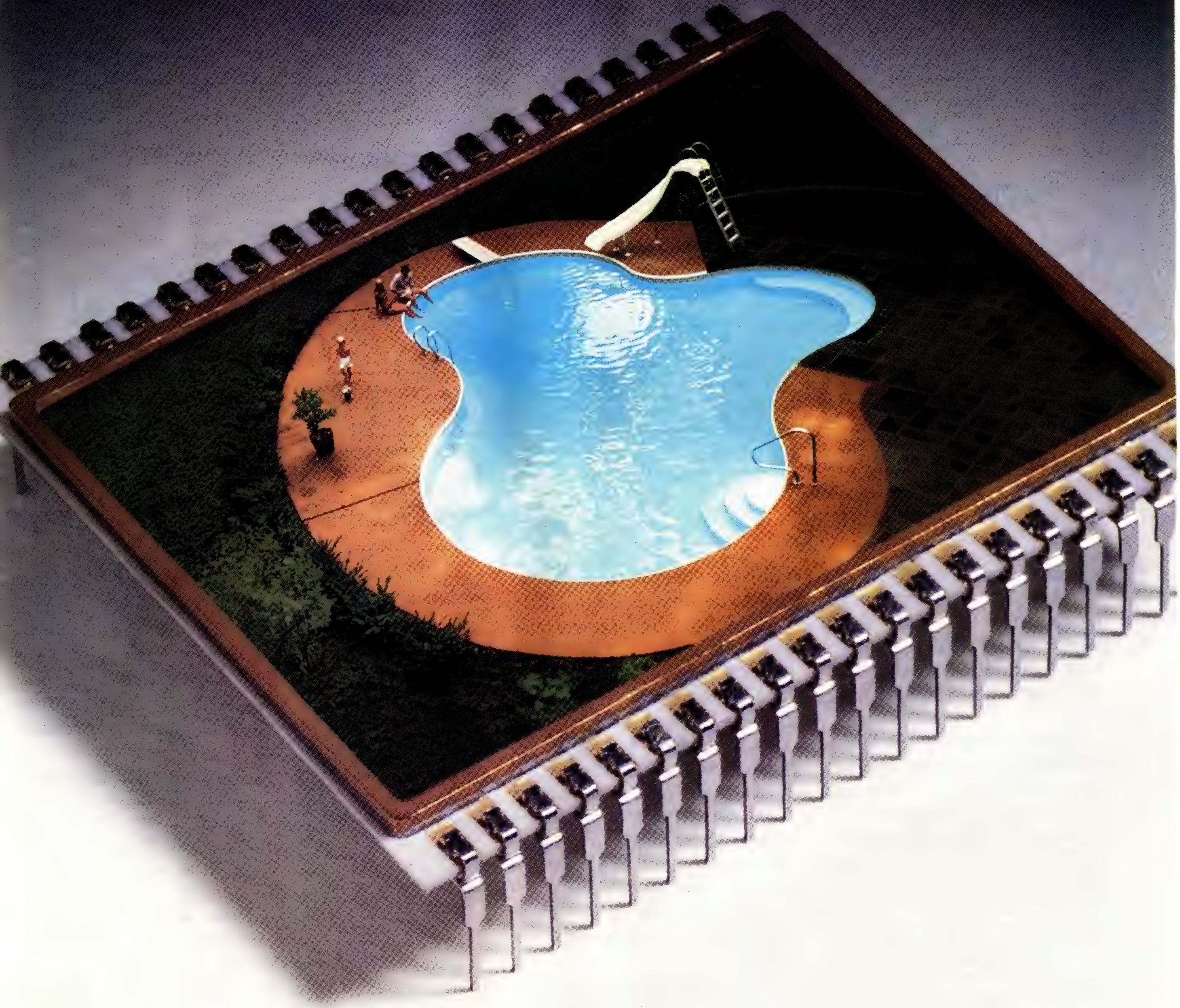

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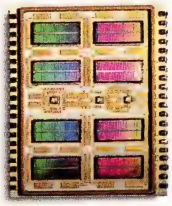

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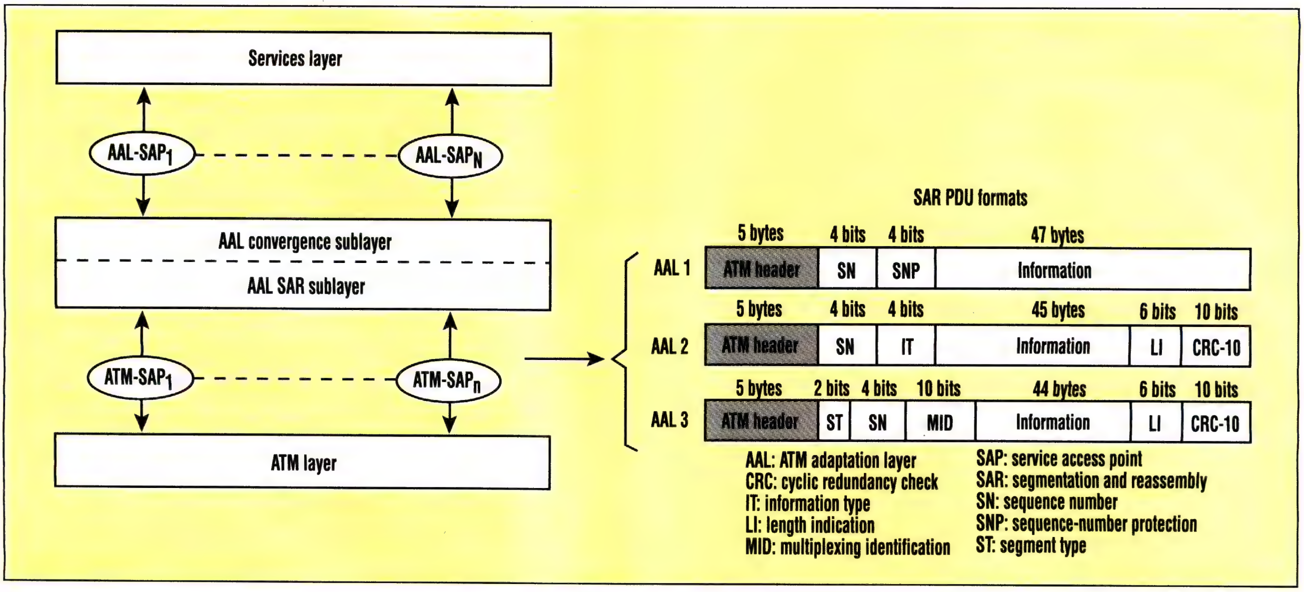

5. Variable-length user service data units are transferred across an AAL service access point for processing by the convergence sublayer and segmentation-and-reassembly sublayer.

vice access point (SAP). The inverse process occurs on the transmitter side. An ATM switch routes user cells via the switch fabric to an output port that's determined by the routing table.

Routing integrity is an important measurement because it ensures that cells delivered to a device's input port are transferred to the appropriate output port or SAP. Each cell's VPI/VCI label determines the output location. So to test an ATM switch, the routing table must be configured to a known condition containing a list of VPI/VCI labels for each input port. The routing path's integrity can then be verified by applying an ATM cell stream to an input port and counting the cells received at the assigned output port.

For complete verification, each switch port must be tested for every VPI/VCI combination. This is a large task, but test time can be reduced by using an automatic test program. Once the routing functions are verified, the performance at the ATM layer must be tested. Cell delay, cell loss, and misinsertion are the important parameters.

Delay is a characteristic of ATM switches because of the buffering used to match the peak input bandwidth to the total available switch bandwidth. Workstations and servers also use buffering when multiplexing various services into the available cell bandwidth. In addition, the cell stream for a particular virtual connection experiences variations in cell interarrival times as idle cells or cells from other virtual connections are inserted. These delays are important because the AAL layer's functions require the cell interarrival times to be within certain limits to effectively process services.

Delay measurements are performed by timestamping the cells transmitted and received by the measuring instrument. The departure timestamp is inserted into the cell payload, and the arrival timestamp is tagged to the received cells. The instrument calculates the difference for each cell and usually displays the results in the form of a histogram *(Fig. 4)*.

For workstation or server measurements, the cells aren't generated by the test equipment and don't contain timestamps. Instead, the interarrival time is calculated using only the arrival timestamp.

The timestamp resolution must be better than the maximum cell repetition rate. A resolution of 100 ns works for measurements at a data rate of up to 622 Mbits/s. But for systems transmitting data at 2.488 Gbits/s, in which the effective width is 0.17 μs, resolution should be boosted at up to about 25 ns.

Cell loss, which also is measured at the ATM layer, can occur for three reasons. First, cells may be discarded by the policing function if the negotiated bandwidth conditions of a virtual connection are exceeded. Second, they may be discarded as a result of congestion in the switch. Third, the transmission-convergence function discards cells with errored headers. When testing a network, a cell-loss measurement may include each type of loss. In design verification, the assumption would be that the transmission-convergence sublayer had already been tested so any cell loss would be only to the ATM layer.

To measure cell loss, an incrementing sequence number is inserted into the payload of a virtual connection (the VPI/VCI label) in the test ATM cell stream. Missing sequence numbers on the receive end are counted as cell losses. Cell loss can be measured as a function of increasing bandwidth to verify the policing function. A zero cell

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loss would be expected for a particular virtual connection until the negotiated bandwidth is actually exceeded.

Designers also should ensure the integrity of the cell payload through a switch. Consequently, routing tests should include a PRBS signal in the cell payload so a payload BER test can be performed simultaneously.

Also specified at the ATM layer are OAM functions for virtual-path (F4) and virtual-channel (F5) connections. Included are fault detection, performance monitoring, and continuity checks. Preassigned header values identify end-to-end and segment F4 and F5 OAM cells. The payload of these cells contains the OAM type (4 bits), function (4 bits), a field whose format is specific to each function (45 bytes), and a CRC10 field (10 bits) for error protection. The remaining six bits, which are reserved for future use, have a default value of 000000.

To verify the OAM functions, designers must simulate all defined formats. Testing these functions also verifies that the ATM layer can multiplex cells from the OAM process on the transmit side and demultiplex the preassigned OAM headers on the receive side.

At the AAL, a separation begins to appear between design verification testing and conformance testing. The interface between the AAL and the services layer occurs at an AAL-SAP. Each type of AAL type has two sublayers, the segmentation-and-reassembly (SAR) sublayer, which is service-independent, and the convergence sublayer (CS), which is service-specific. The CS has two parts, the service-specific CS (SSCS) and the common-part CS (CPCS).

Variable-length user service data units (user-SDUs) are transferred across an AAL-SAP and processed by the CS and SAR sublayer, resulting in fixed-length 48-byte SAR-protocol data units (SAR-PDUs) at the ATM-SAP *(Fig. 5)*. The CS adds a header and trailer to the user-SDU. The resulting CS-PDU is divided into fixed segments and the SAR sublayer adds its own header and trailer to form a SAR-PDU. Each AAL type has unique SAR-PDU formats. The SAR-PDU processing is usually implemented in hardware.

To verify hardware design, it's usually sufficient to test to make sure cells with SAR-PDUs are received error-free and in the correct sequence. Testing the many variations possible within the AAL protocols requires a more complex conformance test approach and is concerned with software aspects of the design rather than the hardware apsects.

To verify the hardware aspects of the AAL layer, the measuring instrument must simulate and monitor the different SAR-PDUs used by each type of AAL. It must also be able to perform sequence-integrity checks and error-performance checks on the equipment transmitter and receiver.

Individual designs will dictate the exact suite of tests that must performed. Once the hardware is proven, designers can begin testing the various software functions associated with such things as services, signalling, performance, and network management.

Ward Carolan, a product marketing engineer for Hewlett-Packard's Australian Telecom Operation, received a bachelor's degree in engineering (electronics) from Swinburne Institute of Technology in Melbourne and a graduate diploma in business management from the Royal Melbourne Institute of Technology.

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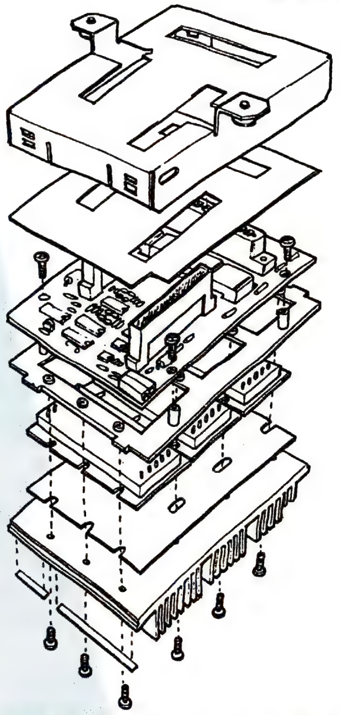

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P. O. Box 1488
Skokie, IL 60076
(708) 677-4700
(CSA) (DSA)
CIRCLE 633

(see p. 142 for key)
(continued on p. 142)

COMMUNICATIONS TEST EQUIPMENT MANUFACTURERS

Microwave Logic
285 Mill Rd.
Chelmsford, MA 01824-4190
(800) 643-2167
(508) 256-6800
(BER) (DPG) (JIG)
(JIM) (TRA)
CIRCLE 634

National Instruments Corp.
6504 Bridge Point Pkwy.
Austin, TX 78730-5039
(512) 794-0100
(DSA)
CIRCLE 635

New Wave Instruments
128 W. 3100 N.
Provo, UT 84604
(801) 373-4909
(CER) (DPG)
CIRCLE 636

Noise Com Inc.
E. 49 Midland Ave.
Paramus, NJ 07652
(201) 261-8797
(BER) (CER) (JIG)
(NOG) (NOT)
CIRCLE 637

Odetics
Precision Time Div.
1515 S. Manchester Ave.
Anaheim, CA 92802
(714) 758-0400
(DTA) (JIM)
CIRCLE 638

Optoelectronics Inc.
5821 N.E. 14th St.
Ft. Lauderdale, FL 33334
(305) 771-2050
(CER) (INT) (ISD) (NWT)
CIRCLE 639

Pacific Electro Data
14 Hughes
Suite B-205
Irvine, CA 92718
(800) 676-2468 or
(714) 770-3244
(PRO)
CIRCLE 640

Photonic Systems Inc.
1800 Penn St.
Suite 4B
Melbourne, FL 32901
(407) 984-8181
(BSA)
CIRCLE 641

Photon Kinetics Inc.
9405 S.W. Gemini Dr.
Beaverton, OR 97005-7160
(503) 644-1960
(FLO) (FOT) (OPM) (OTR)
CIRCLE 642

Pragmatic Instruments Inc.
7313 Carroll Rd.
Suite J
San Diego, CA 92121-2319
(800) 772-4628
(619) 271-6770
(DMT) (NOG)
CIRCLE 643

H. C. Protek Inc.
154 Veterans Dr.
Northvale, NJ 07647
(201) 767-7242
(DPG) (DSA)
CIRCLE 644

Racal Instruments Inc.
4 Goodyear St.
Irvine, CA 92718
(714) 859-8999
(CER) (JIM)
CIRCLE 645

Radcom Equipment Inc.
900 Corporate Dr.
Mahwah, NJ 07430
(201) 529-1100 ext. 260
(BER) (DTA) (ISD) (LAN)
(MWT) (PRO) (WAN)
CIRCLE 646

Rapid Systems Inc.
433 N. 34th St.
Seattle, WA 98103
(206) 547-8311
(BSA) (DPG) (DSA)
CIRCLE 647

Sencore Inc.
3200 Sencore Dr.
Sioux Falls, SD 57107
(800) 736-2673
(JIG) (JIM) (MTR) (TDR)
CIRCLE 648

Sheldon Instruments
P. O. Box 877
Orem, UT 84059
(800) 743-5366
(801) 377-2525
(BSA) (DSA) (NOG)
CIRCLE 649

Simpson Electric Co.
853 Dundee Ave.
Elgin, IL 60120
(708) 697-2260
(NOT) (OPM)
CIRCLE 650

Stanford Research Systems
1290D Reamwood Ave.
Sunnyvale, CA 94089
(408) 744-9040
(DSA) (JIM)
CIRCLE 651

T.A.L. Enterprises
2022 Wallace St.
Philadelphia, PA 19130
(215) 763-2620
(PRO)
CIRCLE 652

TEAM Systems
2934 Corvin Dr.
Santa Clara, CA 95051-0706
(800) 338-1981
(408) 720-8877
(TRA)
CIRCLE 653

Tekelec
26580 W. Agoura Blvd.
Calabasa, CA 91302
(800) 835-3532
(BER) (DTA) (ISD) (LAN)
(PRO) (TRA)
CIRCLE 654

Tektronix Inc.
Communications Test Div.
P. O. Box 1520
Pittsfield, MA 01202
(800) 426-2200
(BER) (BSA) (CER) (CSA)
(DMT) (DPG) (DTA) (FLO)
(ISD) (LAN) (MOA) (MTR)
(OPM) (OTR) (OEC) (TDR)
(TRA)
CIRCLE 655

Telecom Analysis
Systems Inc.
34 Industrial Way E.
Eatontown, NJ 07724
(908) 544-8700
(BER) (CER) (DTA) (ISD)
(JIG) (NWT) (NOG) (TRA)
CIRCLE 656

Telecommunications
Techniques Corp.
20410 Observation Dr.
Germantown, MD 20876
(301) 353-1550
(BER) (BSA) (CSA) (DTA)
(DSA) (FLO) (ISD) (JIG) (JIM)
(LAN) (NWT) (OPM) (OTR)
(PRO) (TDR) (TRA))
CIRCLE 657

Triticom
Box 444180
Eden Prairie, MN 55344
(612) 937-0772
(LAN) (PRO)
CIRCLE 658

Wandel & Goltermann
2200 Gateway Centre Blvd.
Morrisville, NC 27560-9228
(919) 460-3300
(BER) (BSA) (CER) (CSA)
(DTA) (INT) (ISD) (JIG) (JIM)
(LAN) (MOA) (NWT) (NOG)
(NOT) (OPM) (OEC) (PRO)
(TRA)
CIRCLE 659

KEY

(ATM)	ATM test equipment
(BER)	Bit-error-rate testers
(BSA)	Broadband spectrum analyzers
(CER)	Cellular radio test sets
(CSA)	Communication signal analyzers
(DTA)	Digital data transmission analyzers
(DMT)	Digital modulation testers
(DPG)	Digital pulse generators
(DSA)	Dynamic signal analyzers
(FLO)	Fault locators
(FOT)	Fiber-optic testers
(INT)	Interference testers
(ISD)	ISDN test equipment
(JIG)	Jitter generators
(JIM)	Jitter measurement
(LAN)	LAN analyzers
(MOA)	Modulation analyzers
(MTR)	Metallic time-domain reflectometers
(MTS)	Microwave testers
(NWT)	Network test sets
(NOG)	Noise generators
(NOT)	Noise test sets
(OPM)	Optical power meters
(OTR)	Optical time-domain reflectometers
(OEC)	Optical-to-electrical converters
(PRO)	Protocol analyzers
(TDR)	Time-domain reflectometers
(TIA)	Time-interval analyzers
(TRA)	Transmission analyzers
(WAN)	WAN analyzers

▼ 1300-NM FIBER AMP OFFERS +17 DBM OUTPUT

The PFA1000 fiber amplifier operates in the 1300-nm optical-wavelength transmission window. The unit can deliver +17 dBm of optical output power and more than 30 dB of small-signal gain. Pump power is generated by a compact neodymium:YLF laser running at 1047 nm. The amplifier, packaged in a standard EIA/IEC 2U rack-mountable case 16.75 in. wide by 16.60 in. deep, features a complex set of monitor and control functions—including ac power supply, ancillary electronics, and input and output isolators—and requires no periodic adjustments. Suitable applications include studies of 1300-nm digital and analog passive optical networks, research in areas like four-wave mixing and other nonlinear fiber effects, and amplification of tunable ring lasers. The PFA1000 costs $75,000, with delivery in approximately 16 weeks.

Hewlett-Packard Co.
5301 Stevens Creek Blvd.
P.O. Box 58059
Santa Clara, CA 95052-8059
(302) 633-7459
▶CIRCLE 663

▼ FDDI MODULE ENHANCES PROTOCOL ANALYZER

The FDDI application module for the Chameleon Open LAN/WAN protocol analyzer enables users to monitor and simulate FDDI rings. With the FDDI module, the Chameleon Open can test Ethernet, token-ring, WAN (frame relay, X.25, ISDN), SMDS (DS1 and DS3), and ATM networks. The module currently supports SMT 6.2, and there are plans to upgrade it to SMT 7.2 by year's end. The Chameleon Open does integrated, simultaneous testing of LAN, WAN, and broadband networks and applications all in one system. Both portable and rack-mount models are available. The analyzer is based on the Unix operating system and employs a graphical user interface based on the X-Window System and Motif standards. The FDDI application module costs $14,000.

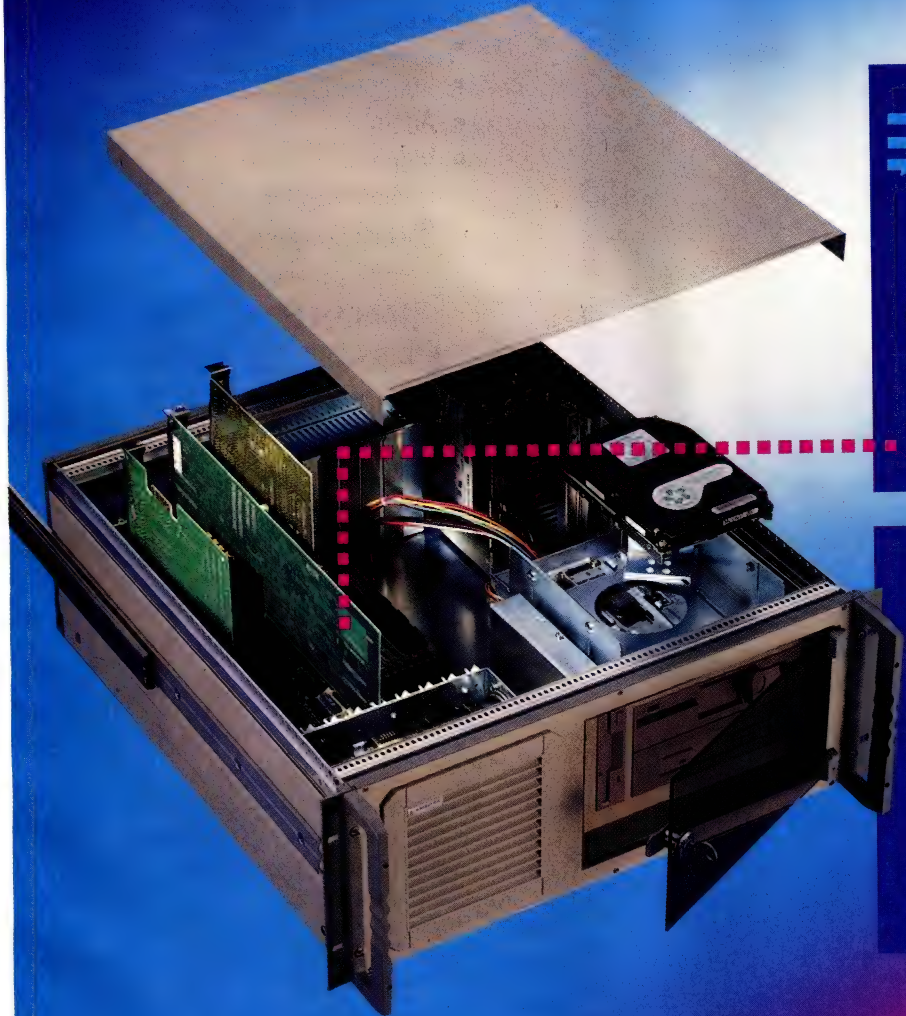
Tekelec
26580 W. Agoura Rd.
Calabasas, CA 91302
(800) 835-3532
▶CIRCLE 664

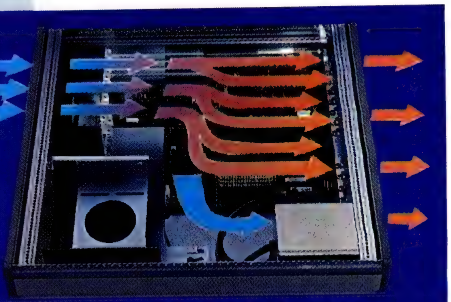
READER SERVICE 109

If your hardware has a hard life.

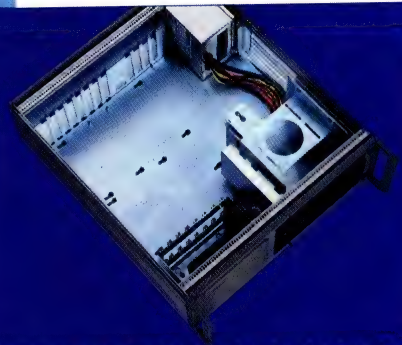
PCs in industrial applications – that's often the real test for toughness. Unless, of course, your PC is packaged in a Chasseleon enclosure. This robust 19" chassis – also available as a bench case – puts your mind at rest, protects your PCs and facilitates installation. All built-in components can be pre-assembled outside the enclosure and then mounted in seconds.

A simple solution for robust protection.





The intelligent thermal-management system is based on forced ventilation. This design ensures functional capability for your electronics and contributes to a low-noise environment.



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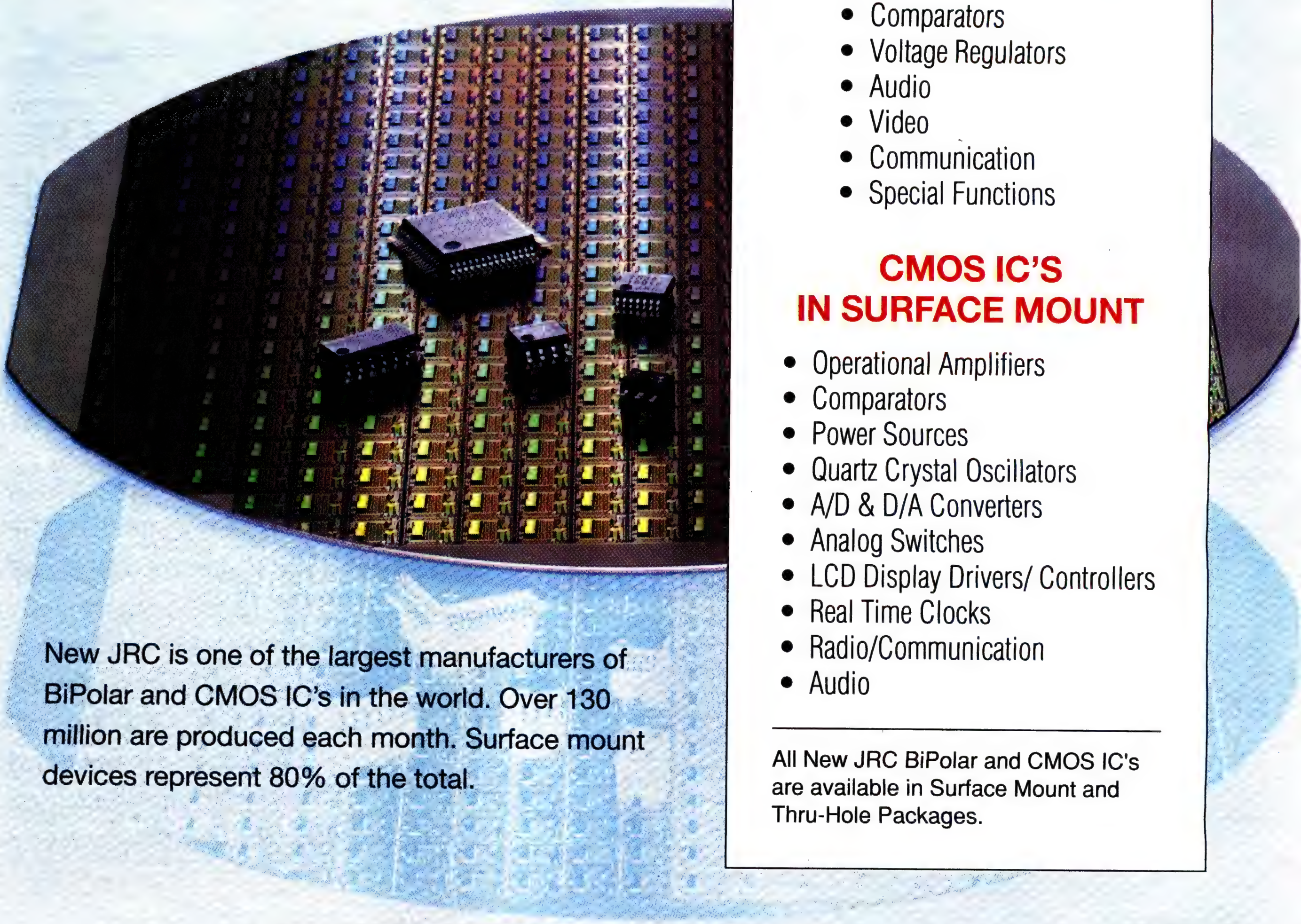

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READER SERVICE 221

▼ HANDHELD LAN TESTER MAKES MULTIPLE CHECKS

A handheld LAN diagnostic tester, the NETcat 800, measures the critical performance characteristics of most LAN installations, including length, near-end crosstalk, attenuation, signal-to-noise ratio, impulse and background noise, and Ethernet traffic. The set uses true time-domain reflectometry to measure cable length, distance to impedance anomalies, shorts, and opens. The system is designed for testing unshielded or shielded twisted pair for 10BaseT, 4- or 16-MHz token ring, and thinnet and thicknet installations. A pass/fail indication rapidly checks a cable's compliance with IEEE-802 guidelines for the physical and data link layers of the OSI network model. The NETcat 800 costs $895.

Datacom Technologies Inc.
11001 31st Pl. W.
Everett, WA 98204
(800) 468-5557 or (206) 355-0590
▶ CIRCLE 550

▼ RF TESTER OFFERS WIDE RANGE OF MEASUREMENTS

The CMS 54 communications service monitor offers an extremely wide array of measurement capabilities for evaluating mobile radio transceivers and base stations ranging from 400 kHz to 1 GHz. The unit contains an RF frequency counter/frequency offset counter, 50-W RF power meter and adjacent-channel power meter, tracking generator, spectrum monitor, signal-to-noise meter, sinad meter, modulation meter, AF voltmeter and counter, distortion meter, DTMF decoder, 20-MHz oscilloscope, and dc ammeter and voltmeter. A built-in synthesizer has 10-Hz resolution and handles am, fm, pm, and multitone modulation schemes. Measurement routines and test data can be stored on a memory card, and hard-copy outputs are made through an RS-232C or Centronics interface. The CMS 54, manufactured by Rohde & Schwarz and sold in the U.S. by Tektronix, costs $13,900, with delivery in eight weeks.

Tektronix Inc.
Test & Measurement Group
P.O. Box 1520
Pittsfield, MA 01202
(800) 426-2200
▶ CIRCLE 551

▼ PC-BASED TDR HEAD OFFERS 35-PS RISE TIMES

With a 35-ps, reflected-rise-time capability, the HL-1100 TDR head can locate discontinuities in very fast designs. The rapid rise times also offer high resolution for determining discontinuities spaced only a few millimeters apart. The TDR head, which has a 17.5-GHz bandwidth, is remotely connected to a National Instruments SCXI mainframe and controlled by a PC. By isolating the head in this way, measurements are less susceptible to the noise generated by most computers, and the head is more easily interfaced with microprobes or inconveniently located connectors. The user controls the TDR head through an intuitive Windows-based virtual instrument panel. The HL-1100 TDR head costs $4995, with delivery in four weeks.

Hyperlabs Inc.
13830 S. W. Rawhide Ct.
Beaverton, OR 97005
(503) 524-7771
▶ CIRCLE 552

▼ HANDHELD T1/FT1 TESTER IS HIGHLY AUTOMATED

The HP 37741A handheld T1/FT1 tester includes an Auto button that automatically detects, synchronizes, and reports status, alarm, and error results with one keystroke. The Auto button's functions include identification of fractional or full T1 facilities; detection of line coding and any alarms being received; measurement of line frequency and level; and detection and reporting of framing, pattern, code, CRC, or BPV errors. The button provides a visual result on the instrument's LCD display and controls its eight bicolor LED indicators, which offer results at a glance. Test results can also be printed out either continuously or periodically through an optional companion battery-operated printer. The HP 37741A runs for four hours on a battery charge. The unit costs $3995.

Hewlett-Packard Co.
Direct Marketing Org.
P.O. Box 58059
MS51L-SJ
Santa Clara, CA 95051-8059
(800) 923-7522
▶ CIRCLE 553

▼ Rb CLOCK LETS COUNTER CALIBRATE COM SYSTEMS

With a rubidium (Rb) atomic clock used as a timebase, the SR625 frequency counter is designed to make traceable frequency calibrations of base stations, transmitters, and many types of communication systems. The instrument directly measures signals up to 2.2 GHz with 12 digits of resolution in a 1-second measurement interval. The Rb timebase has an accuracy of 5×10^{-11}, and a monthly drift of 5×10^{-11}. The SR625 has a 10-min. warmup time. A 10-MHz rubidium output can be used to drive other test equipment, such as spectrum analyzers and synthesizers. The SR625 costs $14,850, with delivery in four weeks.

Stanford Research Systems
1290D Reamwood Ave.
Sunnyvale, CA 94089
(408) 744-9040
▶ CIRCLE 554

▼ MONITOR SYSTEM ACCESSES REMOTE WAN/LAN LINKS

Coupled with an RC-100WL protocol analyzer, the RH-300 access and monitoring system allows any link in a network to be accessed instantly for monitoring and testing. One dial-up modem at a remote site will supply access to all WAN/LAN links attached to the RH-300. Users can set up and define alarm conditions that activate when the defined threshold is exceeded. Up to 1024 links can be monitored at each remote site. The unit accesses multiple interfaces: RS-232, V.35, RS-530, X.21, and a universal module that supports additional interfaces like T1 and LANs. Dual monitor buses permit two circuits to be monitored and tested simultaneously. The average per port price of the RH-300 is $250.

Radcom Equipment Inc.
900 Corporate Dr.
Mahwah, NJ 07430
(201) 529-1100 ext. 260
▶ CIRCLE 555

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COMMUNICATIONS TEST

▼ MODULATION METER TESTS MOBILE COMM EQUIPMENT

With its low residual modulation, true peak detection, and self-calibration capability, the Model 8211 is well-suited for testing of mobile communications equipment. The unit makes am and fm measurements of carriers from 2 to 1500 MHz. The 8211 automatically generates two crystal-controlled frequencies to internally calibrate the fm channels and two separate levels to calibrate the am channel. The result is a mid-range accuracy of 1%. Modulation bandwidth (am and fm) is less than 30 Hz to 15 kHz; am modulation depth is 0 to 100%, and fm deviation is 150 kHz peak. An IEEE-488 interface lets users connect the 8211 to a computer for data transfer or analysis of results. The Model 8211 costs $3100. Delivery is in four to six weeks.

Boonton Electronics Corp.
791 Route 10
Randolph, NJ 07869-1980
(201) 584-1077
▶ **CIRCLE 556**

▼ ANALYZER OPTION ADDS SONET OC-12 TESTING

A Sonet testing option for the T-Berd 310 communications analyzer allows the instrument to generate and monitor OC-12 signals. The option also makes it possible to drop, insert, and analyze DS3 or DS1 (VT1.5) channels from OC-12 access points. With the option, users get section, line, path, and virtual tributary analysis to isolate network problems and error sources from OC-12 down to the DS0 rate. The T-Berd 310's "Thru Mode" operation permits testing of automatic protection switching to verify service restoration, and at the same time provides drop and analysis of lower-rate signals. Ease-of-use features include automatic Sonet/DS3/DS1 frame, pattern, and payload identification; simultaneous results accumulation; and summary results categories.

Telecommunications Techniques Corp.
20410 Observation Dr.
Germantown, MD 20876
(301) 353-1550
▶ **CIRCLE 557**

▼ OPTICAL POWER METER HAS PLUG-IN FLEXIBILITY

The Advantest Q8221 optical power meter features a ±2.5% basic accuracy and a wide selection of plug-in units to measure many lightwave signal parameters. The two channels can be used independently or simultaneously, as well as for channel ratio measurements. Available plug-ins include light sources, detectors, relative intensity noise, optical return loss, high sensitivity (–93 dBm), high power (+27 dBm), and general purpose. To handle various fiber connectors, FC, SC, ST, DIN, SMA, and tape fiber adapters are available for the plug-ins. The units are sold in North America by Tektronix. The Q8221 mainframe costs $1900. Plug-in units range from $750 for the short-wavelength power sensor to $7150 for the 1550-nm laser source. Delivery is in 10 weeks.

Tektronix Inc.
P.O. Box 1520
Pittsfield, MA 01202
(800) 426-2200
▶ **CIRCLE 558**

▼ MOBILE TRANSMITTER TESTER IS VERY FAST

The MS8604A digital mobile transmitter tester measures burst modulation accuracy in less than 1 second, and occupied bandwidth, spurious emissions, and leakage power of adjacent channels in 2 seconds or less. The instrument combines a 100-Hz-to-8.5-GHz spectrum analyzer with a 400-kHz-to-2.1-GHz digital modulation analyzer. Other measurements include frequency error, signal transmission rates, antenna power, and transmission ramp-up and ramp-down power. Storage facilities include internal memory, a plug-in memory card, or an optional floppy drive. The MS8604A costs $68,350. Delivery is in six to eight weeks.

Anritsu Wiltron Sales Co.
685 Jarvis Dr.
Morgan Hill, CA 95037-2813
(408) 776-8300
▶ **CIRCLE 559**

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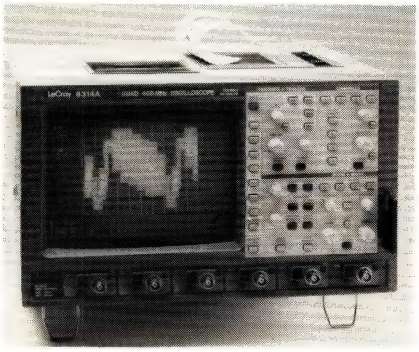
READER SERVICE 204

▼ DSO FAMILY OFFERS UP TO 1-MPOINT MEMORIES

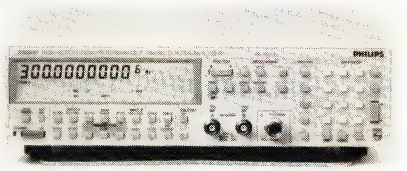
A family of eight 100-Msample/s digital oscilloscopes offers users a wide range of choices. The *9300A* series scopes come in two- and four-channel versions with record lengths of 50 kpoints to 1 Mpoint per channel, and with either 200- or 400-MHz bandwidths. All of the instruments use 8-bit flash converters for digitization. The long acquisition memories ensure excellent timing resolution on any timebase setting. Also, waveforms can be expanded by up to 20,000 times for closer examination. IEEE-488 and RS-232C interfaces are standard. A Centronics printer port is optional, as is a built-in high-resolution graphics printer. Other options include an internal floppy drive and PCMCIA memory-card reader, both DOS-compatible. Prices range from $5990 to $15,740. Delivery is in four weeks.



LeCroy Corp.
700 Chestnut Ridge Rd.
Chestnut Ridge, NY 10977-6499
(914) 425-2000
▶ CIRCLE 560

▼ COUNTER-TIMERS FEATURE EXPANDED CAPABILITIES

Two additions to the PM 6680 family of counter-timer analyzers expand the series' capabilities. The PM 6681 features a time-interval resolution of 50-ps single-shot and 1-ps averaged, and makes up to 8000 measurements/s. The PM 6680B is an enhanced version of the PM 6680. It has 25-ps single-shot and 100-ps averaged resolution and makes up to 2000 measurements/s. The PM 6681 is a 300-MHz unit, and the PM 6680B works to 225 MHz. Both can be expanded to 4.5 GHz. Resolution is 11 digits/s. When the instruments are linked to a PC running the TimeView software package, they become modulation-domain analyzers. TimeView handles time and frequency analysis and advanced statistical and FFT processing. Built-in statistical functions like maximum, minimum, mean, and standard deviation (rms jitter) are available at the touch of a button. In addition, built-in processing in the PM 6681 performs offset, drift, linearization, scaling, or inversion calculations. The PM 6680B costs $1745, and the PM 6681 goes for $2950. TimeView costs $310.



Fluke Corp.
P.O. Box 9090
Everett, WA 98206-9090
(800) 443-5853 (206) 347-6100
▶ CIRCLE 561

▼ PROGRAMMER OPTION ADDS 64 MBYTES OF STORAGE

The optional mass-storage module (MSM) for the UniSite universal programmer supplies 64 Mbytes of nonvolatile, internal bulk data storage. The increased storage capability will allow shorter download times for frequently used data patterns. Also, the MSM permits uncompressed storage of system and algorithm files, thus reducing boot times and increasing operating speeds. Moreover, storing all algorithm files on the MSM eliminates the need to swap between the UniSite system and algorithm floppy disks. A user-installable MSM kit costs $1950. Customers who already own the UniSite software version 4.5 receive a $450 discount. The UniSite programmer with the MSM costs $13,695; the UniSite-68 with the MSM costs $17,895.

Data I/O Corp.
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
▶ CIRCLE 562

▼ 225-MHZ COUNTER MEASURES 12 DIGITS/S

With a measurement speed of 12 digits/s, the HP 53132A 225-MHz universal counter allows for fast, precise benchtop or automated testing. The counter makes more than 200 fully formatted measurements per second. In addition to typical measurements like frequency, period, and time interval, the unit measures pulse parameters, duty cycle, and frequency *ratios*. Built-in statistics and math functions let users display scaled measurement data. An optional third channel measures frequency to 3 GHz. The counter performs automatic limit testing, and can log and flag out-of-limit conditions as well as generate a signal to trigger external devices. An IEEE-488 port and talk-only RS-232 port are standard. The HP 53132A costs $2400 and delivery is in four weeks.

Hewlett-Packard Co.
Direct Marketing Org.
P.O. Box 58059
MS51L-SJ
Santa Clara, CA 95051-8059
(800) 452-4844 ext. 8122
▶ CIRCLE 563

▼ UNIT MEASURES FREQUENCY ERROR USING GPS SIGNALS

The GPStat frequency-error measurement system uses the Universal Coordinated Time signals transmitted by the Global Positioning Satellite system to measure the error in any frequency from 50 kHz to 11 MHz. Typical applications include checking dedicated high-performance oscillators like cesium, rubidium, and quartz devices, and other frequency sources that use Loran C, WWV, or other receivers. An optional Windows interface simplifies operation and supports modem access. The unit comes with an external universal supply that ensures compatibility with power sources throughout the world. The GPStat costs $2995 in single-unit quantities and is available for immediate delivery.

Odetics Precision Time Div.
1515 S. Manchester Ave.
Anaheim, CA 92802-2907
(714) 774-5000
▶ CIRCLE 564

▼ 80C196 EMULATOR HANDLES INTERNAL/EXTERNAL MODE

The EMUL196-PC in-circuit emulator fully emulates both internal and external modes of the Intel 80C196. The PC/AT-based emulator, which uses bondout chips, includes up to 1 Mbyte of shadow RAM, allowing the RAM's contents to be displayed in real time. A Windows interface simplifies operation. The probe, which attaches to the emulator board through a 5-ft. long ribbon cable, plugs into the system under test through adapters. The adapters are available for most 80C196 packages. An optional trace board holds up to 512 krecords and features multiple trigger levels, filtering, and loop counting. The EMUL196-PC costs $1995. Trace boards start at $3300, and pods start at $1995. All are available now.

Nohau Corp.
51 E. Campbell Ave.
Campbell, CA 95008-2053
(408) 866-1820
▶CIRCLE 565

▼ ANALOG INPUT BOARDS HAVE 16-BIT RESOLUTION

The WB-ASC16 series of plug-in boards for IBM PC compatibles, consisting of three models, supply eight channels of 16-bit analog input for a wide variety of input types. The WB-ASC16-TC accepts thermocouple, millivolt, and volt-level signals directly. The WB-ASC16-GP accommodates millivolt or volt-level inputs. And the WB-ASC16-RTD accepts RTD temperature sensors directly. All boards also incorporate eight individually programmable digital I/O channels. Included is icon-driven data-acquisition software that requires no programming to use. In addition, drivers for most common programming languages are supplied. The base unit for the RTD input costs $1209.

Omega Engineering Inc.
1 Omega Dr.
P.O. Box 4047
Stamford, CT 06907-4047
(203) 359-1660
▶CIRCLE 566

▼ 68349 EMULATOR WORKS TO 25 MHZ IN REAL TIME

An HMI-200 series in-circuit emulator for the Motorola 68349 offers real-time emulation at up to 25 MHz. The system features four complex break and trigger points, two 16-ktrace-by-120-bit buffers, 256 kbytes of shadow RAM, and 256 kbytes of overlay RAM expandable to 2 Mbytes. Both 5- and 3.3-V versions of the chip in QFP packages are supported. Included is the SourceGate II emulator control and source-level debugger, which supports all major C and Ada compilers on IBM PC, HP, and Sun platforms. The 68349 emulator starts at $16,000. A hardware-implemented performance analysis option for trace timestamping, software performance profiling, and code coverage analysis costs $2500. Delivery is in two weeks.

Huntsville Microsystems Inc.
P.O. Box 12415
Huntsville, AL 35815
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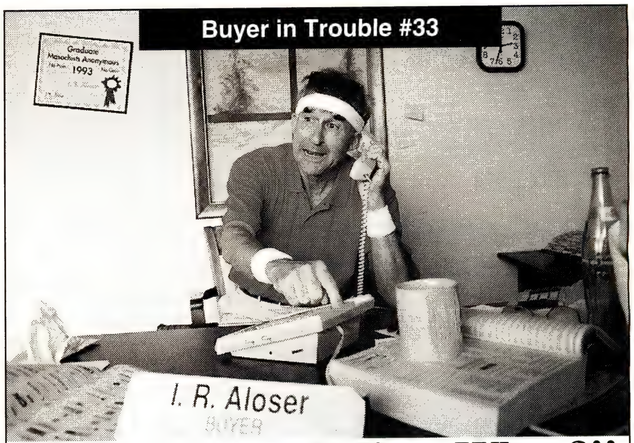

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▼ PC-BASED SCOPES HAVE 300-MHZ BANDWIDTHS

A pair of single-slot PC/AT plug-in boards offer the functionality of 300-MHz digital oscilloscopes with the convenience of a personal computer. The one-channel PCI-425 and two-channel PCI-435 feature 27 timebase settings from 200 ms/div. down to 500 ps/div. in equivalent sampling mode. An automatic trigger-level algorithm quickly establishes a valid trigger level. The boards' 50-Ω inputs make them ideal for ATE systems when testing communication signals, component pulse responses, and fast digital signals. The included BenchCom software contains tools needed to integrate the boards into a test system. The scopes have seven voltage ranges, ac and dc coupling, dc offset, and a probe compensation signal. The optional BenchTop software offers a graphical user interface and the ability to store and recall waveforms and test setups, as well as automate test routines. The PCI-425 costs $1695 and the PCI-435 $2695. BenchTop costs $495. Delivery is in six weeks.

PC Instruments Inc.
9261 Ravenna Rd.
Bldg. B11
Twinsburg, OH 44087-249
(216) 963-0800
▶ CIRCLE 568

▼ 10-W AMPLIFIER COVERS ULTRA-WIDE BANDWIDTH

An ultra-wideband power amplifier, the Model 10W1000A, delivers a minimum of 10 W linear CW power from 500 kHz to 1 GHz. This combination of bandwidth and power is needed in applications that require instantly available full bandwidth without tuning or bandswitching, total immunity to load mismatch, and ample reserve power. Examples include EMC susceptibility testing, antenna and power-meter calibration, and RF heating. A front-panel analog gain control allows for easy setting of output power and adjustment of radiated field strength during shielded-room RF testing. The unit also features advanced protective circuitry and unusually cool operation. The 10W1000A costs $5000. Delivery is in six weeks.

Amplifier Research
160 School House Rd.
Souderton, PA 18964-9990
(800) 933-8181 or (215) 723-8181
▶ CIRCLE 569

▼ SOFTWARE TRANSFERS SCOPE DATA TO A PC

The Waveform Manager software package gives users of Fluke 97 ScopeMeters and Tektronix 222-series digital oscilloscopes an easy way to transfer waveforms and measurements from their scopes to their Windows applications. Users can pull several waveforms into a picture, drag them into position, resize them, add notes, and copy the picture through the clipboard to other applications without creating a file. The package also operates as a standalone program with monochrome or color-printer support, waveform file management, and cursor measurements. The program converts waveforms to user-configurable data tables readable by spreadsheets and math programs. The software runs on 386 or better PCs under Windows 3.1. Waveform Manager costs $279 and is available from stock.

Metratek
33688 N. W. Bagley Rd.
Hillsboro, OR 97124
(503) 693-1607
▶ CIRCLE 570

▼ 84C13/15 EMULATOR HAS SOURCE-LEVEL DEBUGGER

The UEM-8400 in-circuit emulator supports all four versions of the Zilog 84-series processors—the 84C13, 84C15, 84C013, and 84C015—with one pod. The instrument comes with a Windows-hosted source-level debugger. Also included is a performance analyzer that simultaneously monitors the time spent in up to 255 routines with an accuracy of better than 100 ns. A 4-ktrace buffer generates views of the data as raw machine instructions, C source, or mixed C and disassembled code. Triggers qualify trace data to collect only that which is needed. The emulator includes 131,072 hardware breakpoints. Breakpoints also can be set on data values. In addition, complex breakpoints with five-level-deep conditions are supported. The UEM-8400 costs $5500 and is available from stock.

Softaid Inc.
8310 Guilford Rd.
Columbia, MD 21046
(800) 433-8812
(410) 290-7760
▶ CIRCLE 571

▼ 50-W SUPPLY FEATURES TWO SEPARATE OUTPUTS

The HP E3620A dual-output dc power supply offers two independent 0-to-50-V, 50-W outputs in a compact, lightweight, and economical package. The instrument specifies both normal-mode voltage noise and common-mode current noise, and 0.01% load and line regulation keep the output steady with changes in the load and power line. Separate digital panel meters allow users to monitor both outputs simultaneously. The outputs are protected against overloads and short-circuit damage. The HP E3620A dual-output power supply costs $500.

Hewlett-Packard Co.
Direct Marketing Org.
P.O. Box 58059
MS51L-SJ
Santa Clara, CA 95051-8059
(800) 452-4844 ext. 8185
▶ CIRCLE 572

▼ PC-BASED DIGITAL TESTER CHECKS LOADED BOARDS

The ICT-32 is a digital in-circuit tester used to find faulty devices on loaded printed-circuit boards. The unit can test ICs with up to 28 pins using a DIP clip. The tests involve forcing the device's inputs (backdriving upstream devices) and then sensing the device's outputs. The system includes an IBM PC-compatible plug-in card, a pod, and DIP clips. Individual ICs can be tested out-of-circuit through a ZIF socket mounted on the pod. Libraries of test files cover over 95% of devices, including 7400, 5400, 4000, 4500, 4700, and 7500 series ICs and interface ICs in TTL and CMOS. The ICT-32 costs $895.

International Science Corp.
2556 Massachusetts Ave.
Cambridge, MA 02140
(617) 876-5278
▶ CIRCLE 573

▼ TOOL VERIFIES IC'S COMPLIANCE WITH 1149.1

The AVLsim Tool Kit uses logic simulation to verify that IEEE-1149.1 boundary-scan hardware has been implemented correctly. The tool is well-suited for both chip- and board-level environments. After the boundary-scan verification, the logic simulator can be used to generate test vectors automatically, so that test programs can be written and debugged before hardware exists. AVLsim creates stimulus patterns for all popular logic-simulation tools and works with any logic simulator that accepts tabular stimulus from a test file. It also is suitable for use with hardware simulators and emulators from Quickturn, Pi, IKOS, and Zycad. The DOS version of AVLsim is available immediately, starting at $6000 for a single-seat license.

Alpine Image Systems Inc.
821 Riverside Dr.
Los Altos, CA 94024
(415) 941-3247
▶CIRCLE 574

▼ VXI ARCHITECTURE GIVES ATE SERIES FLEXIBILITY

The Aurora series of fully integrated, turnkey automated test systems uses a VXIbus architecture to reduce ATE development times and the costs of system design, integration, and debugging. The series comes in three basic versions—the VTS-1000, VTS-2000, and VTS-3000—that can be adapted to become virtually any kind of ATE system. Included are a 486-based, 33-MHz controller; a hard drive; a 15-in. VGA monitor; and keyboard and trackball capabilities. Standard software supplies a visual test environment that displays test equipment front panels and totally paperless manuals and documentation. Prices vary from under $100,000 to approximately $175,000, depending on configuration. Delivery is in 18 weeks.

ManTech Test Systems
12015 Lee Jackson Hwy.
Fairfax, VA 22033-3300
(703) 218-6400
▶CIRCLE 575

▼ CHARACTERIZE DEVICES TO FEMTOAMP LEVELS

The RI-2000 dc device characterization system incorporates a switchable 8-pin low-noise matrix that allows the unit's four high-precision voltage and current sources to supply accurate power to the device under test (DUT). A 16-bit digital multimeter and high-precision matrix-resident picoammeter allows users to measure performance from femtoamperes to amperes. The system uses a 486-based controller, with data-acquisition software that permits any matrix line to source or monitor the DUT without changing connections. Built-in utilities help users rapidly develop device-specific test plans. The system can be expanded to become a full dc parametric tester. The RI-2000 costs $34,500, with delivery in five to seven weeks.

Reedholm Instruments Inc.
47810 Westinghouse Dr.
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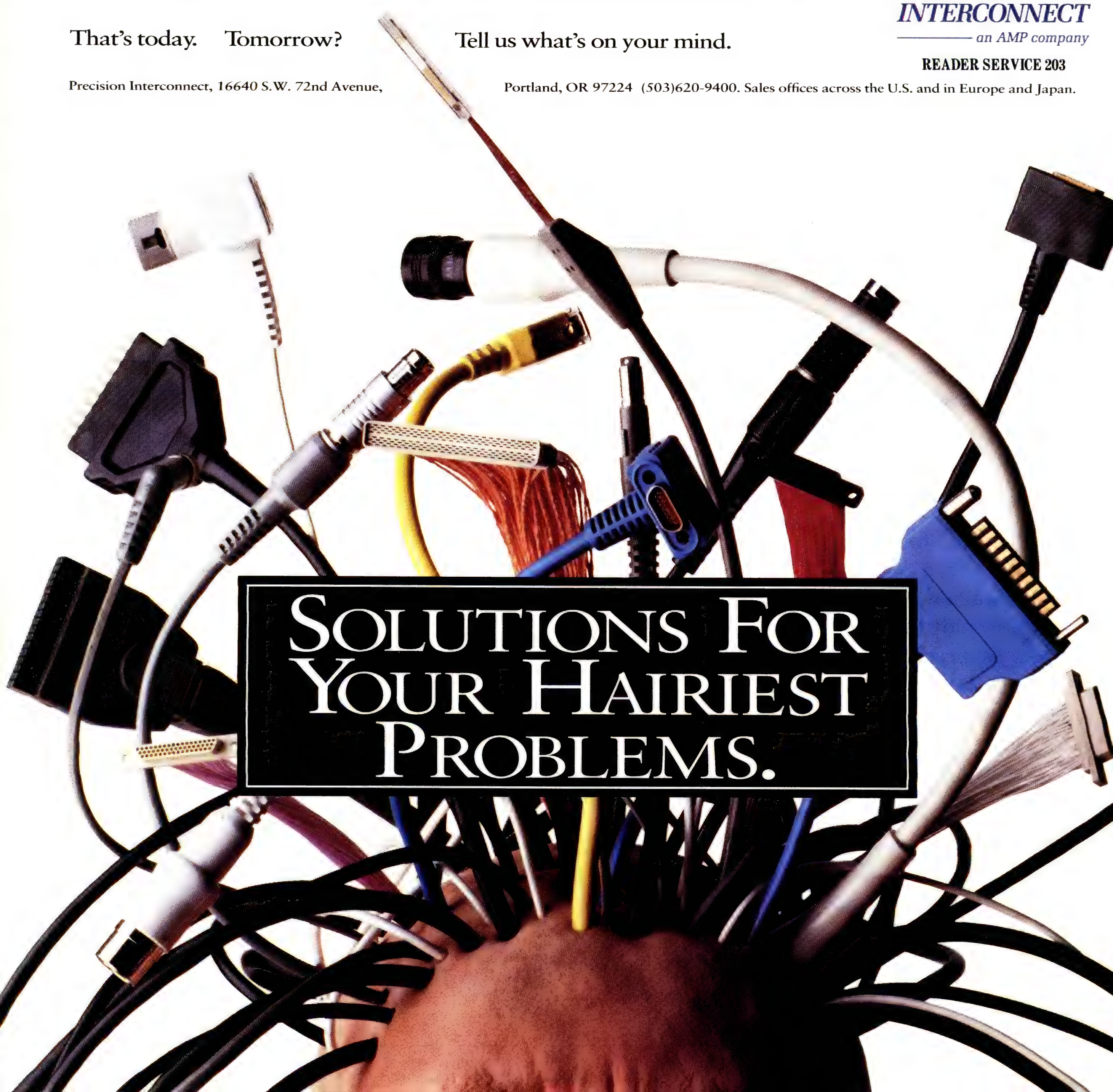

A SPECIAL EDITORIAL FEATURE

PIPS

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ELECTRONIC DESIGN

Adopting Multichip-Module Technology

Going to MCMs isn't as scary as it seems anymore.

BY SHIV C. TASKER

Cadence Design Systems Inc., 270 Billerica Rd., Chelmsford, MA 01824; (508) 262-6104.

and ZORAN SEKULIC

Integrated Measurement Systems Inc., 9525 S.W. Gemini Dr., Beaverton, OR 97005; (503) 626-7117.

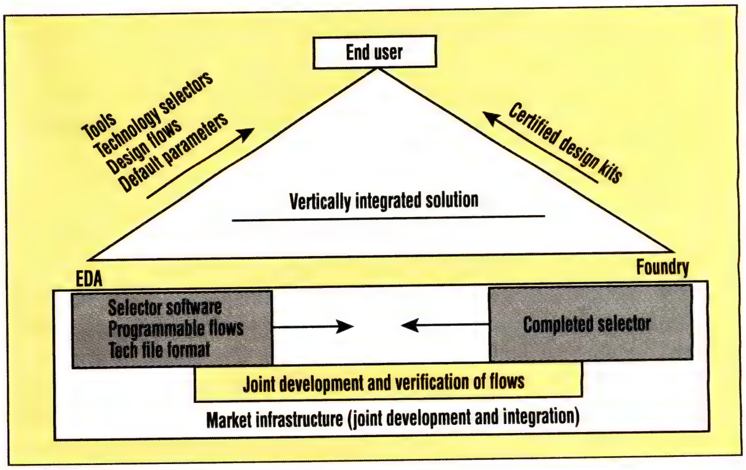
Differentiating your products from everyone else's is getting tougher to do. In an environment where hardware margins keep dropping, the pressure on engineers to deliver products that can be clearly differentiated is immense. After all, the earlier you can bring a unique product to market, the more you can charge for it. Unfortunately, in the almost perfect market in which we find ourselves, everyone can access almost the same technologies. Therefore, the engineer's task of creating a better lure is more difficult than ever.

One possibility for gaining a competitive edge is through the use of multichip-module (MCM) technology. In a world where smaller, denser, and faster is better, MCMs offer a tidy way to achieve all three attributes. The last few years have seen considerable hype surrounding MCMs, with overly aggressive estimates as to when the technology would become widely used commercially.

But as is often the case, reality has taken hold. Early adopters of MCM technology found that implementation was more difficult than they thought. The good news is that these early implementation efforts focused attention on issues that will benefit all of us in the long term. These issues, among others, included the lack of an industry infrastructure to address MCM design, fabrication, assembly and test, the supply of known-good die (KGD), and the end users' lack of MCM experience.

MCMs come in various substrate technologies, which include laminate (MCM-L), ceramic (MCM-C), deposited thin films (MCM-D), and hybrids of the latter two (MCM-C/D). There also are various approaches to mounting die on a common substrate, such as flip-chip, wire bonding, TAB, BGA, and SMT. Before end users can choose intelligently from among these substrate and chip-attach options, it's essential that they have a clear idea of the benefits they're looking to derive from their MCM implementation. This will guide the selection of the appropriate technology at the desired cost point.

For example, high-performance system applications like telecommunications, workstations, file servers, and multimedia may find MCM-D more suitable for their markets, even though the technology may be more expensive. Applications such as automotive, portable PCs, disk drives, and cellular phones are primarily looking for size and weight benefits. These applications also are an order of magnitude higher in volume shipments with a lower price ceiling, dictating a much lower cost point. In this case, MCM-L using thin dielectrics is more appropriate. Special applications, including military/aerospace or medical, may not fall into either of these categories—they may



1. MCM foundries, EDA vendors, and test companies are forging alliances intended to minimize the risk of adopting MCM technology. The ultimate goal is to push the rate of adoption past that of such technologies as SMT or ASICs.

TABLE 1: EXAMPLES OF MCMs

Application	Company	Product	Description
Mainframe	IBM	ES/9000	MLC MCM-D/C
	Unisys	A16/A19	Multicavity ceramic PGA
	Siemens	7500	MCL-L with flip TAB
Mid-range computer workstation	IBM	AS/400	MLC with flip chip
	NCR	3500	Laminate with TAB
	Control Data	4680	nChip's thin-film process
	Tadpole Technology	SPARCbook	nChip's thin-film process
	Silicon Graphics	Iris	Four-chip ceramic PGA
	IBM	RS/6000	MLC with flip chip
PCs	Austek Micro.	486 upgrade	MicroModule Systems' thin film on aluminum
	IBM	9095	Four-chip ceramic MCM
Telecom	AT&T	Many	PolyHIC thin-film process
	PMC	Sonet	Thin film on silicon
	NEC	Sonet	Two-sided glass ceramic
Communication	Matsushita	Pager	Laminate MCM
Automotive	Mercedes-Benz	Mercedes	Four-chip, two-sided LTCC from MPA
Military	Rockwell	DSP	Thin film on silicon
	Hughes	Processor	Thin film on alumina (HDMI)
	Honeywell	Processor	Cofired ceramic MCM
Consumer	Matsushita	VCR	MCM-D for CCD driver ICs
Medical	Medtronics	Defibrillator	MLC

Source: TechSearch International Inc.

MCMs offer a tidy way to achieve smaller, denser, and faster end products, thereby giving you a competitive edge.

be after greater reliability and better thermal dissipation and heat removal, in addition to the volumetric size reductions, are already realized. For now, MCM-C may be more appropriate for these applications.

Whatever the industry segment, there are clear examples of MCMs in use today *(Table 1)*. IBM Microelectronics Corp., East Fishkill, N.Y., ships an average of 4000 MCMs per week.

Like all new technologies, there have been a number of barriers preventing the wholesale adoption of MCM technology in all designs. There are ways around each of these barriers, albeit with differing degrees of effectiveness. KGD, or at least well-tested die, now are appearing from a number of major silicon vendors. Test can be addressed through a combination of design tools and methodologies, and by effectively using test stations instead of large, costly ATE systems.

One barrier that can't be addressed by vendors, however, is the perception of MCMs as an expensive technology. In many instances, the overall cost of a given system is lower with an MCM implementation than if the system was built with discretely packaged ICs. However, this must be assessed on a case-by-case basis. Consider IBM's application of MCM-C technology in its AS400 Midrange Computer F70. The 64-mm-by-64-mm, 43-layer module carries 15 ICs and 512 signal I/Os. Its total power dissipation is 53 W. The shorter nets reduced path delays for improved performance and substantially lowered overall costs by enabling the board carrying the module to be much simpler and less costly to manufacture.

Among the more interesting developments in increasing the rate of MCM implementations involves the advent of vertically integrated solutions. In the past, the captive foundries of large, vertically integrated companies provided a one-stop shop of services, education, design, fabrication, and, in some cases, assembly and test. A similar level of service is provided by alliances between foundries, electronic-design-automation (EDA) vendors, and test companies *(Fig. 1)*. The end objective is the same: educate the end user of the advantages and risks of adopting MCM technology, minimize those risks through consulting, and deliver foundry-specific optimized design and test solutions that shorten the learning curve. By minimizing the technology risk and by providing services to reduce the process risks, these alliances hope to encourage MCMs' adoption at a somewhat more aggressive pace than was seen with such technologies as surface mounting or ASICs.

For example, engineers from IBM and Cadence have worked together to share an understanding of the MCM manufacturing process and the design tools. Out of this study, tool efficiencies were identified to make it easier to design for IBM's various types of manufacturing technologies. Cadence provided IBM with software that creates a "flow" or recommended methodology for end users to follow in the design of an MCM. Following this flow ensures that no important steps will be forgotten, that tool parameters are set for optimum execution for the size of the given MCM and its chosen technology, and that libraries of information on cross sections and materials are readily available and need not be created by the end user. With vertically integrated solutions, the end user gets a certified design kit that consists of tools, technology selectors, design flows, and default parameters for the tools that will yield highly manufacturable designs.

One of the most important considerations for engineers, whether they're developing a chip, ASIC, or MCM, is the need to design within the context of packaging hierarchies and types. Unlike an ASIC, where the input and output to the circuit inside the chip is well defined in the form of an I/O

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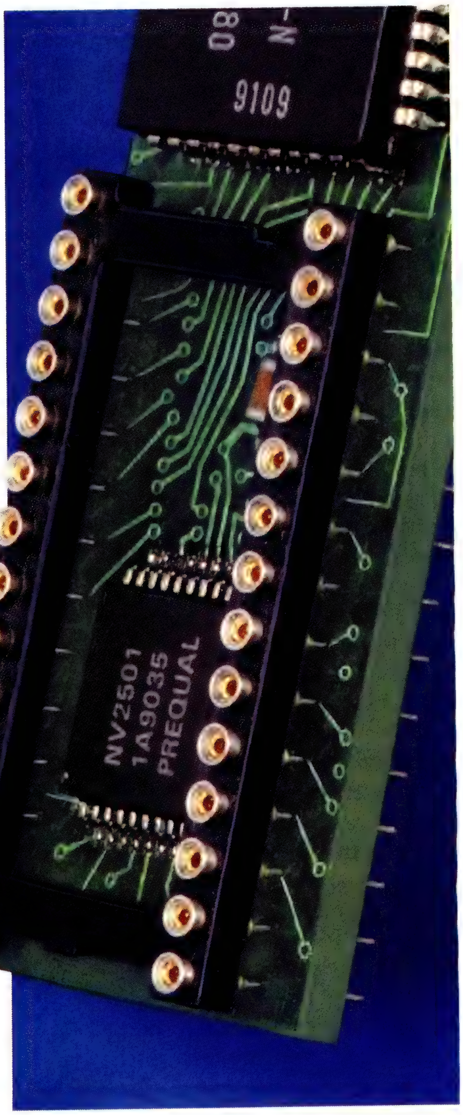

THE PROBLEM:

"We had a bunch of new designs but couldn't get the ICs we needed. Some had excruciating lead times. Some thru-hole parts were obsoleted by surface mount devices. We had new designs plus a huge inventory of existing boards. But we couldn't produce any of them because we couldn't get the right devices.

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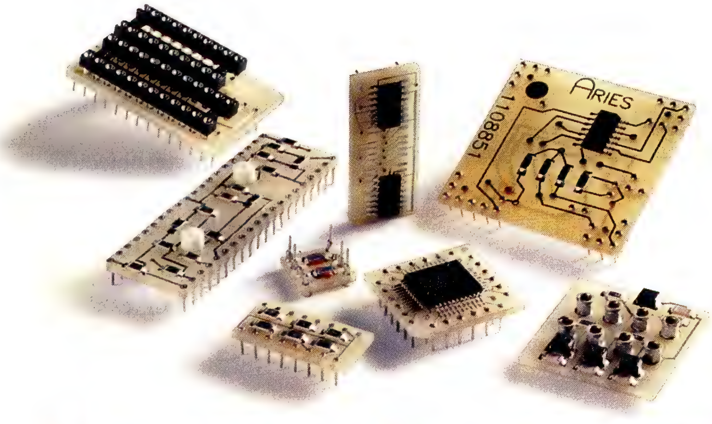

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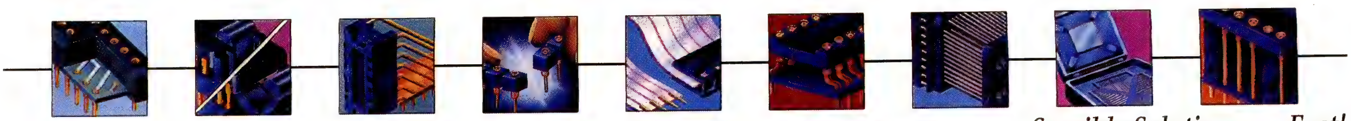

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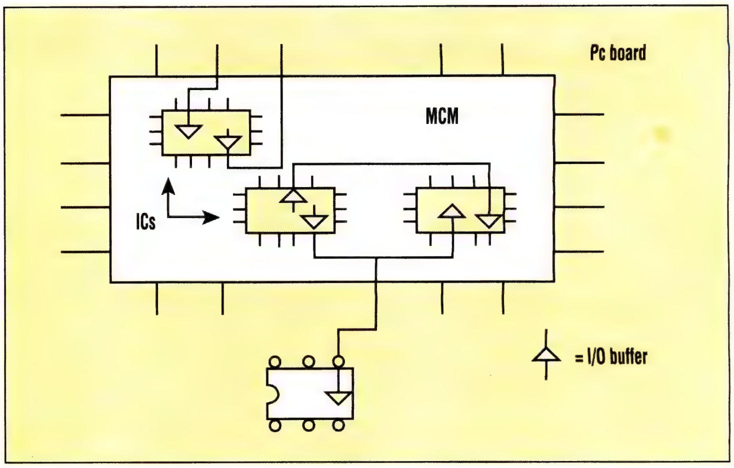
buffer, no I/O buffer exists at the periphery of an MCM. And, if you're looking to MCMs for increased performance, the likelihood of having high-speed circuits between the MCM and the pc board is very high *(Fig. 2)*. Therefore, it's important to design the MCM in the context of the board that will carry the rest of the circuitry.



2. A critical consideration in the design of an MCM is the lack of an I/O buffer at its periphery. Unlike an ASIC, where the input and output to the circuit inside the chip is well defined in the form of an I/O buffer, there's no such buffer in an MCM.

One way of tackling this challenge is through a structured design approach. The MCM is a black box at the schematic level of the pc board, but it can be hierarchically exploded into its constituent elements and packaged individually for the MCM design. Furthermore, signals can be divided into three categories: those that are fully contained on the MCM, those that leave the module through its I/O pins to drive receivers on the pc board, and those that drive receivers on both the MCM and the pc board. The latter class of signals should be kept to a minimum. Signals that stay within the confines of the MCM give you the opportunity to reduce the drive of the buffers on the chip, which yields other benefits like lower power dissipation.

Finally, it's important to use a good signal-integrity tool that can analyze the entire network—both the MCM and the pc board—simultaneously. This will allow you to make decisions regarding the type and placement of terminations, determine the topology for the interconnections both on the MCM and on the board, and provide optimum circuit performance for the entire system instead of just the module.

When using an "off-the-shelf" MCM part, which is to say a commercially available component that uses MCM packaging to integrate a required function, signal-integrity models are the best option. With the industry-standard IBIS initiative, vendors can supply you with the behavioral models you need for signal-integrity timing analysis, without the vendor disclosing proprietary details of their manufacturing technology. Because every signal-integrity vendor has pledged their support and is shipping IBIS-compatible tools, there should be no excuses on the part of the component suppliers.

Considerable confusion has surrounded the simulation strategies for MCMs. For many people who came to MCMs from the IC/ASIC side, there was a belief that simulating a MCM would stress the capacity and speed of commercially available simulators to the point of uselessness. In addition, many thought that putting an MCM on the bench to test it for functionality and to rework connections when mistakes are discovered was difficult. However, unlike the ASIC model, a fully simulated net list isn't a prerequisite for a successful MCM design.

The complexity of simulating an MCM is no different from that of simulating a pc board. If the MCM has more than ASICs on the substrate, a number of modeling methods are required. And, by implication, various simulators are required as well. These different models and simulators must be plugged into some form of a backplane so that they can work together. For example, if the MCM consists of a microprocessor, memory, and a couple of ASICs, the microprocessor may be available as a VHDL model or a hardware model may have to be used, the ASICs may be in Verilog, and there may be some C code.

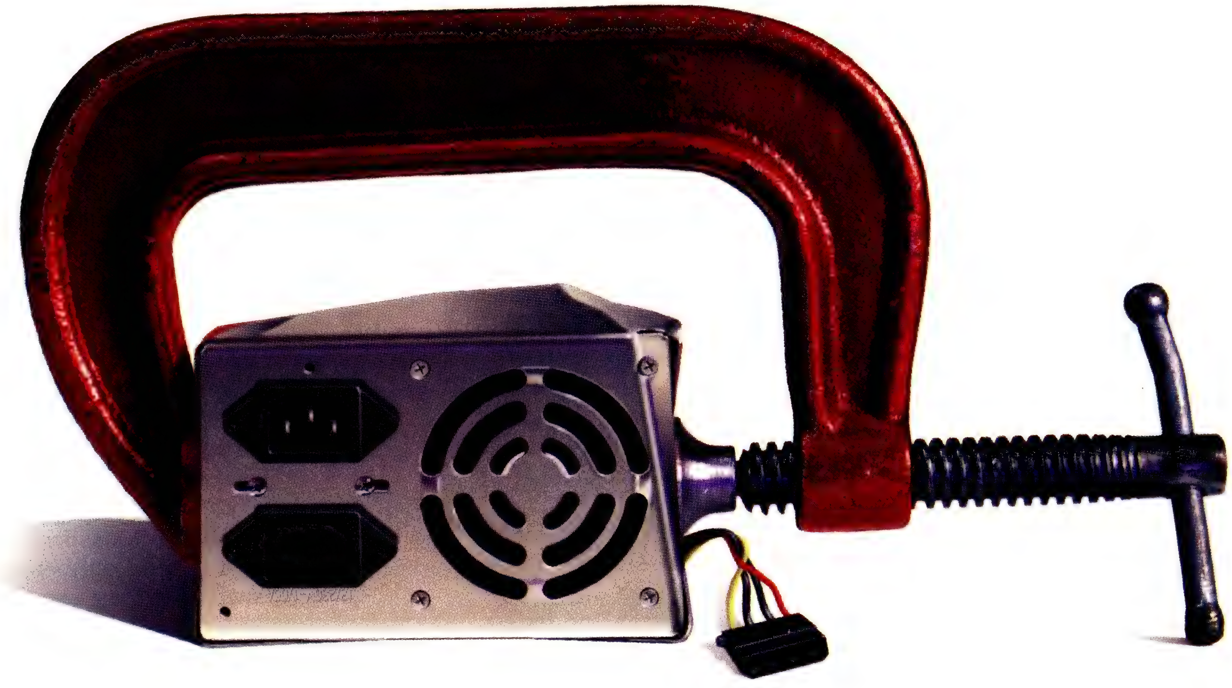
Logic simulation at the MCM level is useful, but if the MCM consists of big building blocks, such simulation may not provide the bang for the buck. It's much more relevant to look for a solution that can provide functional verification with timing analysis and where the critical paths on both the MCM and the host pc board can be examined in totality. As always, timing is the key.

If the ultimate objective for the MCM is to meet performance goals, it's important that those goals not be compromised during the layout process. This means that slack times should be calculated and assigned to nets, so that the placement and routing will meet those constraints. Using a correct-by-design tool can cut many iterations out of the layout-and-analyze cycle.

It's equally important not to

TABLE 2: DESIGN-FOR-TESTABILITY (DFT) TECHNIQUES

Design	Feature
IC design	Boundary scan (IEEE 1149.1) Scan variations (LSSD, etc.) Built-in self-test (BIST)
Circuit design	Partitioning and synchronization Boundary scan
Module design	Boundary-scan options (interconnect, component test)
Substrate layout	Internal test points for access External test pins for access
Simulation	Fault simulation



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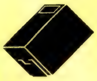
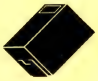
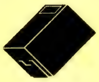
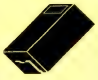
										
6.3 V	10 V		16 V		20 V		25 V		35 V	
330 µF	220 µF	100 µF	100 µF	47 µF	68 µF	33 µF	33 µF	22 µF	22 µF	10 µF/15 µF
100 mΩ ESR	100 mΩ ESR	100 mΩ ESR	100 mΩ ESR	150 mΩ ESR	150 mΩ ESR	200 mΩ ESR	200 mΩ ESR	300 mΩ ESR	300 mΩ ESR	300 mΩ ESR
D case size = EIA 7343 E case size = EIA 7343H										

READER SERVICE 238

overly constrain the layout. Because everything is closer together on an MCM, the parallel paths are much smaller and may be less than the saturation length. Another tactic is to classify signals into "active" and "sensitive" categories. This lets nets that aren't sensitive run parallel for greater distances than the more susceptible nets during that clock phase.

Because of the lack of a buffer, it may be necessary to defer decisions regarding the placement of terminating resistors until it can be done with the target pc board. When using a hot chip, reflected wave switching is a legitimate technique for reducing thermal dissipation. Therefore, if the MCM must interface with a bus such as the PCI-bus, signal analysis and layout must go hand in hand until the design is done.

Testing is recognized as a crucial MCM issue. MCM test is challenging for a variety of reasons. For one, the packaging's density makes it difficult to gain physical access for fault isolation and repair. For another, the designs' complexity demands the use of design-for-testability (DFT) tools. Moreover, the cost of module assembly and repair encourages use of only KGD in construction. The high performance and high pin counts typical of MCMs stretch the limits of traditional test equipment and methodologies. And, because MCMs often break new ground in performance, function, and assembly techniques, there are no universally-accepted test methodologies, and few test solutions are guaranteed to meet every need.

Such open issues place a burden on the user to understand and select the appropriate test methodology and test process. Those who adapt and implement the right solutions stand to reap the benefits of this innovative packaging technology.

Traditional test techniques for assemblies rely on information obtained through physical contact with internal nodes. MCMs are an order of magnitude denser than what can be supported with the best in-circuit test fixtures. MCM technology has reached densities and complexities that call for test methodologies to be chosen and applied during the design stage. Small geometries, passivations and coatings, hidden traces, flip-chip technologies, cavity-down packaging, and ball-grid arrays are some of the obstacles that can be made "testable" by using more DFT and by non-contact test techniques.

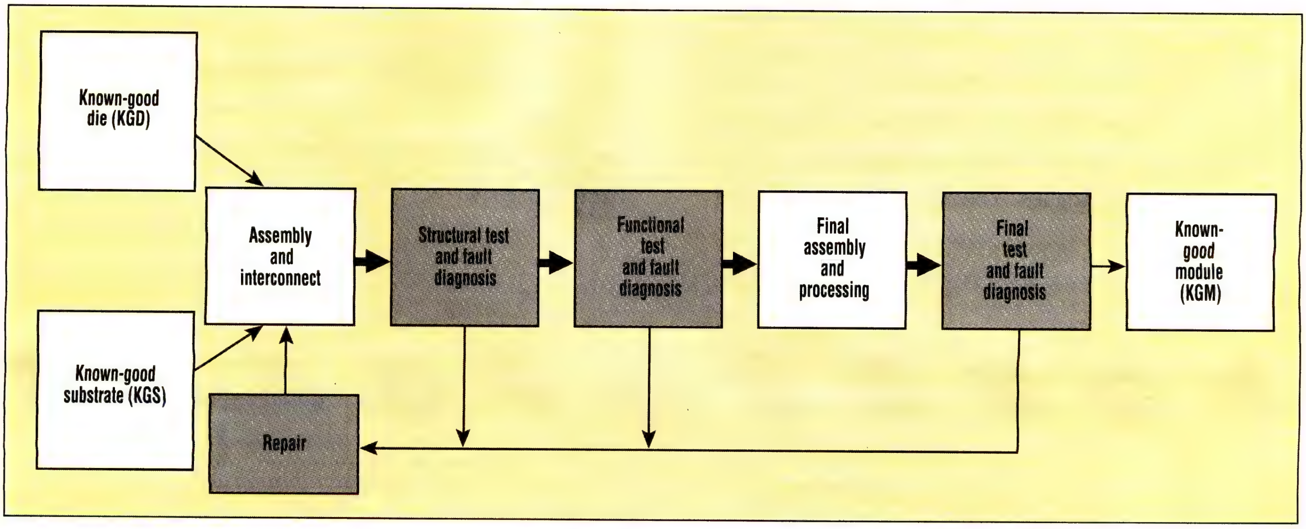
The fundamental difference between MCMs and other packaging technologies is the absolute requirement for DFT and lack of routine physical access for probing. Fortunately, a number of DFT techniques are available to facilitate the test process *(Table 2)*.

MCM manufacturers must produce defect-free modules in a cost-effective fashion. The MCM process consists of alternating assembly and test steps *(Fig. 3)*.

Structural tests like those shown in Figure 3 confirm that the module is correct by construction. The best example of structural test is the interconnect test based on the IEEE 1149.1 boundary-scan standard. Structural tests identify failures that depend only on assembly, such as wrong components or bad wire bonds. Such faults comprise most of the assembly faults. The advantages of structural tests are their independence from circuit functionality and complexity, their lack of a requirement for test vectors, and accurate fault isolation. Needless to say, structural tests form the foundation for MCM testing *(Fig. 4)*.

Modern boundary-scan tools, such as Teradyne's VICTORY, provide complete vector generation and fault-isolation techniques for circuits with boundary-scan components. Such boundary-scan components are available today from Analog Devices, AT&T, Brooktree, IDT, Intel, Motorola, TI, and Xilinx, among others.

The key benefits of boundary scan are interconnect test and


Known-good die (KGD)
Assembly and interconnect
Known-good substrate (KGS)
Repair
Structural test and fault diagnosis
Functional test and fault diagnosis
Final assembly and processing
Final test and fault diagnosis
Known-good module (KGM)

3. MCM assembly and test includes both structural tests to check construction and functional tests to check behavior. Structural tests, such as boundary scan, are the foundation for MCM fault isolation.

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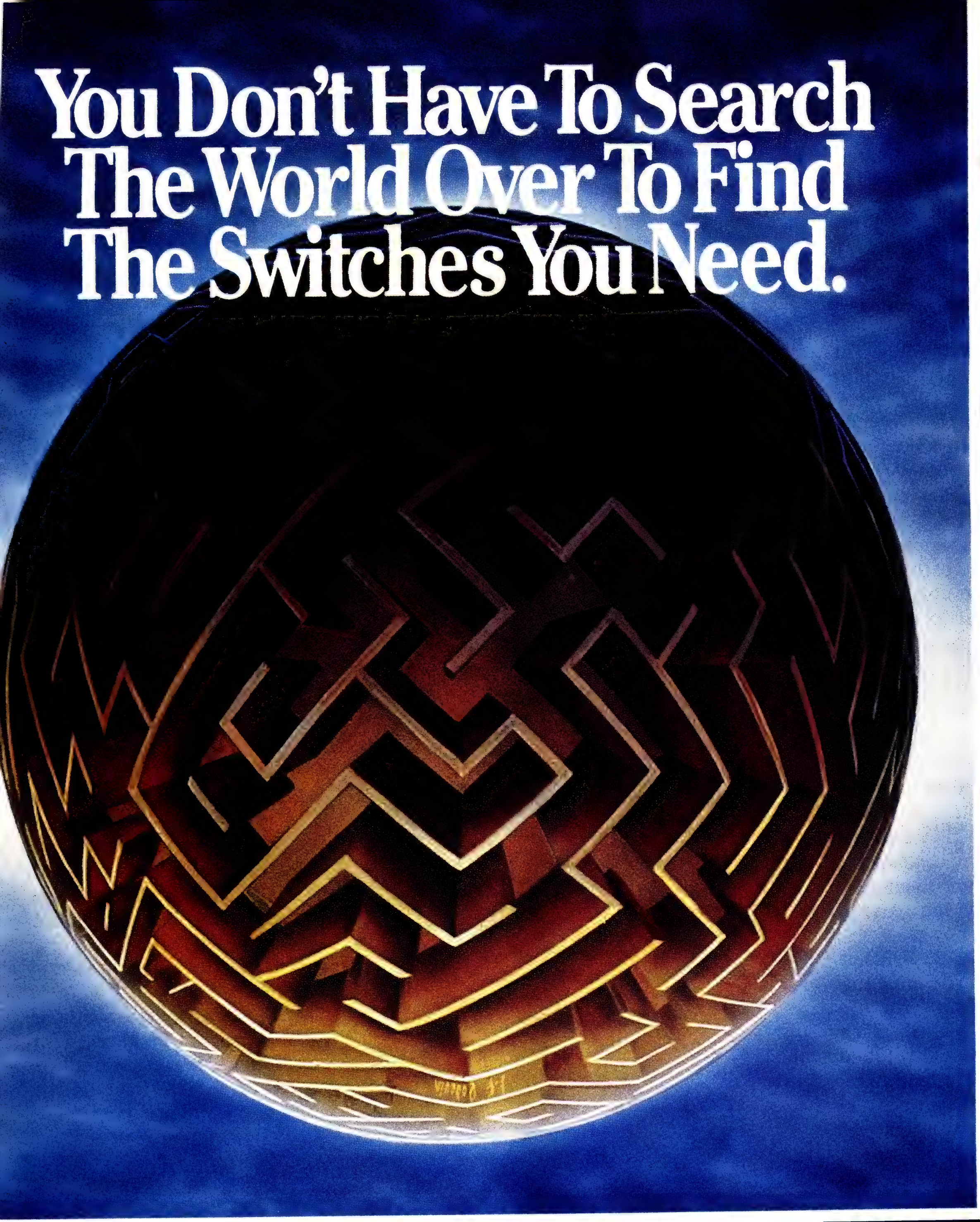

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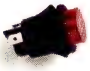

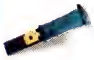

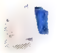

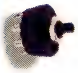

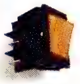

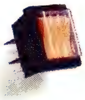

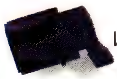

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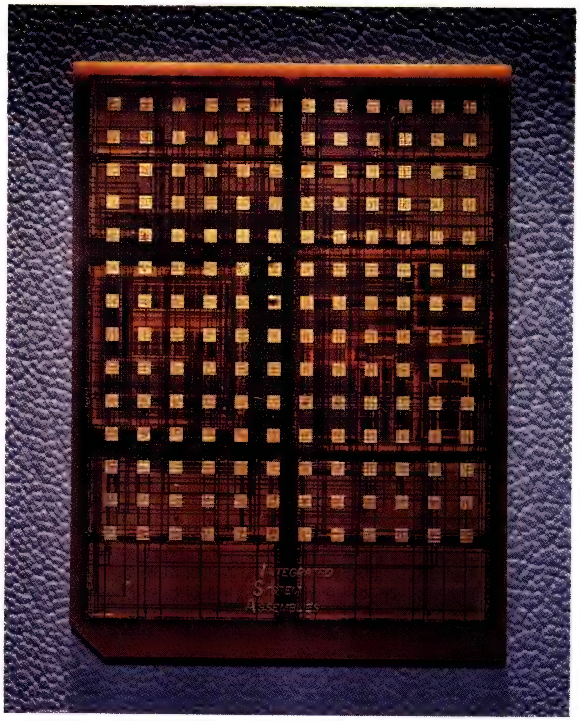

4. With conductors patterned on top of the die, the SuperSPARC AMCM module achieves excellent performance but requires DFT for access. Photo courtesy of Integrated Systems Assemblies Corp.

component test. Virtual Interconnect Test (VIT) provides full ATPG and 100% pin-level coverage for interconnects between boundary-scan components. Virtual Component/Cluster Test (VCCT) enables testing of non-scan components or clusters. VCCT uses the adjacent component boundary-scan pins as virtual tester pins. Clusters and components often require primary (external-I/O) parallel patterns. VCCT automatically synchronizes parallel patterns from the tester-I/O channels with the patterns sent through the boundary-scan path.

Functional tests compare the expected I/O behavior to the actual module response. They identify parametric problems, such as deviations in device speed, interdevice timing problems, transmission-line problems in the substrate, and other defects that can't be checked with the structural test. At-speed tests verify that modules conform to the specifications. Advantages of functional tests include versatility and reuse of simulation vectors.

The availability of KGD is considered the single most important requirement for the MCM industry's growth. Such die have been thoroughly tested and provide an excellent ingredient for MCMs. That's because subsequent tests can concentrate on assembly faults instead of internal die faults.

Active suppliers of tested die include Intel, Micron, Motorola, and National Semiconductor. Die processors such as Chip Supply provide quality components and necessary advice. The key to getting KGD is working closely with the die suppliers on specs, burn-in, and handling.

Adopting a test methodology is frequently more cost-effective than developing your own by process of trial and error. A robust test methodology can be structured on consecutive "inside-out" steps. The vital four "I"s of MCM test are *Ingredients, Interconnects, Interactions,* and *Interfaces*:

- To assure the quality of the *Ingredients*, KGD are required before die placement.
- Boundary-scan test is needed to check the *Interconnects* and device-interconnect continuity.
- Functional test is needed to verify full-speed functionality and device *Interactions.*
- External-pin parametric test enables checking of the primary I/O pins and the ability to *Interface* to the next package level.

MCM test is a top-down activity. MCM testability issues must be recognized early and addressed by adding design-for-testability features at the design level. Assembly processes and test equipment must be selected to match the test methodology and technical requirements of each particular device. While many of these challenges require new thinking about the test process, cost-effective methodologies and tools already exist for manufacturers who understand their test choices.

Test-system alternatives include benchtop instruments, multiple logic analyzers, VXI systems, "hot mock-up" (the system itself), test systems built in-house, ATE, and test stations. These alternatives must be investigated with respect to such attributes as cost, access, pin count, timing accuracy, fixturing, simulation vector translation, throughput, versatility, and ease of maintenance. Versatility is vital for a small company or a department that must find a single tester for all die and module test needs. Can one avoid purchasing test equipment and simply plug the module into the system itself? Just because a processor MCM boots up when plugged into a system doesn't mean that every processor module will work in every system. Test systems are process control tools that can track data and ensure consistent quality.

To summarize, there are paths around all of the major barriers inhibiting the adoption of MCM technology. With the selection of an experienced MCM foundry as a partner/consultant, a vertically integrated design solution targeted for that foundry's process technology, and a carefully planned implementation, MCMs can offer the competitive edge needed by systems designers. Though MCM costs, design solutions, and infrastructure have all improved, designers must still be aware of the KGD issues and the end-user learning curve.

Shiv C. Tasker, vice president and general manager of the Systems Physical Group with Cadence Design Systems Inc., holds a BS in statistics and economics and an MBA from the University of Texas at Arlington.

Zoran Sekulic, product marketing manager at Integrated Measurement Systems Inc., received BSEE and Master of Engineering degrees from Cornell University, Ithaca, N. Y.

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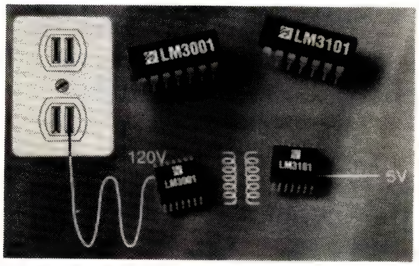
(see p. 169 for key)
(continued on p. 164)

▼ POWER-SUPPLY CHIP SET OPERATES AT 1 MHZ

An off-line switching-power-supply chip set comprises the LM3001 primary-side driver and LM3101 secondary-side controller. Operating at 1 MHz, the chips are claimed as the first monolithic, high-frequency, magnetic-feedback solution for off-line switchmode supplies. The chips provide the control and drive circuitry for isolated off-line supplies using magnetic ac feedback from output to input rather than optical feedback. Used with an external MOS power transistor, the chips form a full switcher. Both come in 14-pin DIP and SO housings. In lots of 1000, pricing is \$1.60 and \$1.80 for the LM3001 and \$1.45 and \$1.65 for the LM3101 in DIPs and SOs, respectively.



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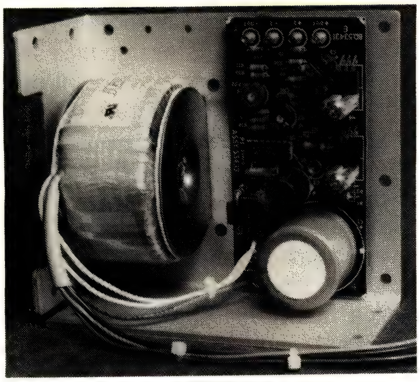

The high reliability of an open-frame linear power supply is enhanced by the use of toroidal transformers, which lend increased efficiency, lighter weight, lower temperature rise, less creepage distance, and lower leakage current than conventional transformers. Models are available with outputs from 5 to 28 V dc and up to 280 W can be special ordered. As an example of pricing, a 5-V dc, 6-A model with over-voltage protection goes for $72.50 in lots of 25. Delivery is in six to eight weeks.

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▼ CURRENT-SOURCE MODULES ANCHOR CHARGERS

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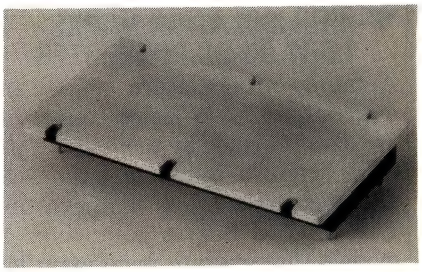

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(617) 245-5900
(BM) (CM) (GP) (IN) (MP)
(RA) (EA)
CIRCLE 735

Ablestik/EMCA-REMEX
National Starch
& Chemical Co.
160 Commerce Dr.
Montgomeryville, PA 18936
(215) 855-1000
(EN) (IK) (TF)
CIRCLE 736

ESP Inc.
14 Blackstone Valley Pl.
Lincoln, RI 02865-1145
(800) 338-4353
(FL)
CIRCLE 737

Electrical Insulation
Suppliers
300 N. Mannheim Rd.
Hillside, IL 60162
(708) 547-5400
(EM) (ER) (FR) (GK) (SE)
(TB) (VE) (WN) (CE) (CC)
(EL) (EN) (EP) (EA) (PF) (FP)
(FE) (FL) (IK) (LA) (MM) (PM)
(RE) (SA) (SO) (SU) (TF)
CIRCLE 738

Electro-Space Fabricators
Inc.
300 W. High St.
Topton, PA 19562-0067
(610) 682-7181
(CN) (CM) (GP) (MI) (RA)
(VR)
CIRCLE 739

Electronic Solutions
6790 Flanders Dr.
San Diego, CA 92121
(619) 452-9333
(BM) (CN) (CM) (EM) (GP)
(MI) (RA) (VR)
CIRCLE 740

Elma Electronic Inc.
44350 Grimmer Blvd.
Fremont, CA 94538
(510) 656-3400
(CM) (EM) (GP) (IN) (MP)
(MI) (PT) (RA) (VR) (WT)
(ER) (GK)
CIRCLE 741

Enclosure Technologies Inc.
256 Airport Industrial Dr.
Ypsilanti, MI 48198
(313) 481-2200
(CM) (PT) (RA)
CIRCLE 742

Enthone-OMI Inc.
P.O. Box 1900
New Haven, CT 06508
(203) 799-4904
(ER) (FL)
CIRCLE 743

Epoxy Technology Inc.
14 Fortune Dr.
Billerica, MA 01821
(508) 667-3805
(EN) (EA) (PM)
CIRCLE 744

Equipto Electronics Corp.
351 Woodlawn Ave.
Aurora, IL 60506
(708) 897-4691
(BM) (CN) (CM) (EM) (GP)
(IN) (MI) (RA) (VR)
CIRCLE 745

Flex Products Inc.
2793 Northpoint Pkwy.
Santa Rosa, CA 95407
(707) 525-7926
(ER) (LA) (SU)
CIRCLE 746

GE Plastics
One Plastics Ave.
Pittsfield, MA 01201
(413) 448-7110
(EL) (EP) (FP) (RE)
CIRCLE 747

Gardiner Metal Co.
Div. of Gardiner Solder Co.
4820 S. Campbell Ave.
Chicago, IL 60632
(312) 847-0100
(FL) (SO)
CIRCLE 748

General Devices Co. Inc.
1410 S. Post Rd.
Indianapolis, IN 46239
(317) 897-7000
(CM) (EM) (GP) (MI) (PT)
(RA) (VR) (ER) (MG) (VE)
CIRCLE 749

Glasteel Industrial
Laminates
P.O. Box 910
Collierville, TN 38027
(901) 853-5070
(LA)
CIRCLE 750

Glenmarc Manufacturing
Inc.
25661 Hillview Ct.
Mundelein, IL 60060
(708) 540-0100
(EN) (EA) (IK) (PM) (RE)
CIRCLE 751

Graseby Plastic Systems
Inc.
261 Cedar Hill St.
Marlboro, MA 01752
(508) 485-7390
(ES)
CIRCLE 752

Haewa Corp.
4357-B Park Dr.
Norcross, GA 30093
(404) 921-3272
(CN) (CM) (GP) (PT) (RA)
(VR)
CIRCLE 753

Heraeus Inc.
Cermalloy Div.
24 Union Hill Rd.
West Conshohocken, PA
19428-9306
(610) 825-6050
(EA) (FL) (IK) (SO) (TF)
CIRCLE 754

Hirose Electric USA Inc.
2688 Westhills Ct.
Simi Valley, CA 93065
(805) 522-7958
(WT) (ER)
CIRCLE 755

Hoechst Celanese Corp.
Advanced Materials Group
26 Main St.
Chatham, NJ 07928
(201) 635-4198
(RE)
CIRCLE 756

HumiSeal
P.O. Box 445
Woodside, NY 11377
(718) 932-0800
(CC)
CIRCLE 757

Hybricon Corp.
12 Willow Rd.
Ayer, MA 01432
(508) 772-5422
(BM) (CN) (CM) (IN) (MP)
(PT) (RA) (VR) (ES) (ER)
CIRCLE 758

I.M.R. Corp.
Microelectronic Research
11132 E. Edison St.
Tucson, AZ 85749
(602) 749-1920
(MP) (ES) (ER) (CE) (CC)
(EN) (EA) (IK) (PC) (PM) (TF)
CIRCLE 759

Imtec Inc.
One Imtec Lane
Bellows Falls, VT 05101
(802) 463-9502
(FP) (FE) (IK) (LA)
CIRCLE 760

(see p. 169 for key)
(continued on p. 166)

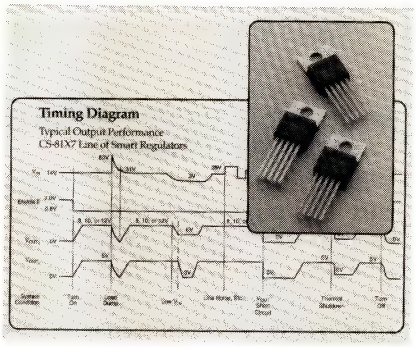
▼ HIGH ISOLATION MARKS 1.5-W DC-DC CONVERTER

A family of miniature single- and dual-output 1.5-W dc-dc converters are distinguished by their 8-kV p-p (4 kV dc) input-to-output isolation level and wide operating temperature. The 100VFI Series comprises 18 models that operate from input levels of 5, 12, or 15 V dc while providing output combinations of 5, 12, 15, ±5, ±12, or ±15 V dc. Other features include high efficiency, low leakage current, and low output ripple and noise. All models include input filtering to reduce reflected ripple current. Packaging is in a 1.27-by-0.80-by-0.40-in. DIP-compatible, 24-pin case. Pricing starts at $25.90 in lots of 100. Delivery is from stock to four weeks.

Conversion Devices Inc.
15 Jonathan Dr.
Brockton, MA 02401
(508) 559-0880
▶ CIRCLE 669

▼ SMART REGULATOR ICs OFFER VERSATILITY

A three-member family of dual-output linear voltage-regulator ICs delivers a wide array of logic-control functions, low quiescent-current sleep modes, and a broad range of output-voltage levels. Each provides a tightly regulated primary output (±2.5%) with a 5-V secondary output for powering CPUs, memories, and logic circuits. Primary output voltages for the CS-8167, CS-8147, and CS-8157 regulators are 9, 10, and 12 V, respectively, at an output current of 500 mA. Secondary 5-V outputs source up to 70 mA. All three offer a CMOS-compatible Enable pin that controls both output voltages. When that pin is brought high under CPU control, the regulators go into sleep mode with a quiescent current draw of 70 µA. These regulators offer designers two tightly regulated voltage levels in one IC while conserving space on printed-circuit boards and holding down current draw. Three variations of the five-lead TO-220 plastic package are available for each family member: straight lead, vertical lead for upright mounting, and horizontal lead for mounting to pc boards. Pricing for all three is $1.18 in lots of 10,000. Small quantities are delivered from stock.



Cherry Semiconductor Corp.
2000 S. County Trail
E. Greenwich, RI 02818
(800) 272-8121
▶ CIRCLE 670

PACKAGING AND MATERIALS MANUFACTURERS

Indium Corp. of America
1676 Lincoln Ave.
Utica, NY 13502
(315) 853-4900
(SO)
CIRCLE 761

Instrument Enclosures
4088 South K St.
Tulare, CA 93274
(209) 688-1100
(CM) (EM) (IN) (MI) (PT) (WT)
CIRCLE 762

Instrument Specialties Co.
P.O. Box A, Broad St.
Delaware Water Gap, PA 18321
(717) 424-8510
(ES) (ER) (GK) (MG) (SE)
(TB) (VE) (EL) (EA) (SA)
CIRCLE 763

Interlogic Industries
85 Marcus Dr.
Melville, NY 11747
(516) 420-8111
(CM) (RA)
CIRCLE 764

Johnson Matthey Inc.
Materials Technology Div.
10080 Willow Creek Rd.
San Diego, CA 92131
(619) 566-9510
(MP) (EA) (SO)
CIRCLE 765

Knurr USA, Inc.
1890 N. Voyager Ave.
Simi Valley, CA 93063
(805) 526-7733
(BM) (CN) (CM) (EM) (GP)
(IN) (PT) (RA) (VR) (WT)
(ES) (ER) (EP) (LA)
CIRCLE 766

Kycon Cable & Connector
1810 Little Orchard St.
San Jose, CA 95125
(800) 544-6941
(CM) (EM) (GP) (PT) (ER)
(FR) (GK) (CE) (EP) (SU)
CIRCLE 767

Kyocera America Inc.
Microelectronics Div.
1740 Technology Dr.
Suite 490
San Jose, CA 95110
(408) 437-8777
(CM) (MP) (CE)
CIRCLE 768

Lanxide Electronic Components
1300 Marrows Rd.
Newark, DE 19714
(302) 456-6300
(MP) (MI) (RA) (MC)
CIRCLE 769

Loctite Corp.
North American Group
705 N. Mountain Rd.
Newington, CT 06111
(203) 280-1280
(CC) (EN) (EA) (PM) (RE)
CIRCLE 770

Magnetic Shield Corp.
740 N. Thomas Dr.
Bensenville, IL 60106
(708) 766-7800
(PT) (MG) (MM)
CIRCLE 771

Markel Corp.
P.O. Box 752
Norristown, PA 19404
(610) 272-8960
(TB)
CIRCLE 772

Master Bond Inc.
154 Hobart St.
Hackensack, NJ 07601
(201) 343-8983
(ER) (CC) (EL) (EN) (EA)
(PM) (RE) (SA)
CIRCLE 773

Miller-Stephenson Chemical Co.
55 Backus Ave.
Danbury, CT 06810
(203) 743-4447
(ER) (CC) (EA) (RE)
CIRCLE 774

Mitech Corp.
1780 Enterprise Pkwy.
Twinsburg, OH 44087
(216) 425-1634
(ES)
CIRCLE 775

Multicore Solders
1751 Jay Ell Dr.
Richardson, TX 75081
(214) 238-1224
(FL) (SO)
CIRCLE 776

NELCO
3 Elm St.
Walden, NY 12586
(914) 778-2111
(LA) (SU)
CIRCLE 777

Olin Conductive Materials
Olin Electronic Materials
1496 E. Francis Ave.
Ontario, CA 91761
(909) 947-2228
(ER) (TF)
CIRCLE 778

Omega Shielding Products Inc.
1384 Pompton Ave.
Cedar Grove, NJ 07879
(201) 890-7455
(ER) (GK) (MG) (SE)
CIRCLE 779

Optima EPS
2166 Mountain Industrial Blvd.
Tucker, GA 30084-5088
(404) 496-4025
(CN) (CM) (EM) (GP) (IN) (MI)
(RA) (VR) (ER) (GK)
CIRCLE 780

PFT Inc.
Hwy. 16 West
Monon, IN 47959
(800) 558-7297
(BM) (GP) (IN) (RA) (VR)
CIRCLE 781

Pacific Microelectronics Corp.
10575 S.E. Cascade Blvd.
Portland, OR 92223
(800) 622-5574
(CM) (MP) (MI) (WT) (CE)
(SU) (TF)
CIRCLE 782

Pacific West Electronics
1370 Logan Ave., Suite A
Costa Mesa, CA 92626
(714) 957-3158
(ER) (FR) (RC)
CIRCLE 783

Palo Alto Design Group
360 University Ave.
Palo Alto, CA 94301
(415) 327-9444
(CM) (GP)
CIRCLE 784

Panel Controls Corp.
1000 Mt. Elliot
Detroit, MI 48207
(313) 568-2400
(RA) (VR)
CIRCLE 785

Parker Seal
Conductive Products
P.O. Box 11751
Lexington, KY 40512
(800) 272-7537
(ER) (GK) (EL) (SA)
CIRCLE 786

Penstock Inc.
520 Mercury Dr.
Sunnyvale, CA 94086-4018
(408) 730-0300
(CM) (MP) (MI)
CIRCLE 787

Permagile Industries Inc.
Insulcast Div.
101 Commercial St.
Plainview, NY 11803
(516) 349-1100
(EL) (EN) (EA) (PM) (RE)
CIRCLE 788

(see p. 169 for key)
(continued on p. 168)

PACKAGING AND MATERIALS MANUFACTURERS

Plaskon Electronic Materials
A Rohm & Haas Co.
Independence Mall West
Philadelphia, PA 19105
(215) 592-2095
(EN)
CIRCLE 789

Plastic Systems
261 Cedar Hill St.
Marboro, MA 01752
(508) 485-7390
(ES)
CIRCLE 790

Pneumafil Corp.
Metal Products Div.
4500 Chesapeake Dr.
Charlotte, NC 28297
(704) 399-7441
(CN) (CM) (EM) (GP) (MI)
(RA) (VR) (WT) (ES) (ER)
(GK)
CIRCLE 791

Powerbox Inc.
1720 14th St.
Boulder, CO 80302
(303) 444-1461
(IN)
CIRCLE 792

Premier Metal Products Co.
381 Canal Pl.
Bronx, NY 10451
(718) 993-9200
(BM) (CN) (CM) (EN) (GP)
(IN) (PT) (RA) (VR)
CIRCLE 793

Pulizzi Engineering Inc.
3260 S. Susan St.
Santa Ana, CA 92704-6865
(714) 540-4229
(BM) (CM) (EM) (GP) (MI)
(PT) (RA) (VR) (ER)
CIRCLE 794

Qualitek International Inc.
315 Fairbank St.
Addison, IL 60101
(708) 628-8083
(FL) (SO)
CIRCLE 795

Quantum Materials Inc.
9938 Via Pasar
San Diego, CA 92126
(619) 695-1716
(EA)
CIRCLE 796

Quartzite Processing Inc.
6 Holyoke St.
Malden, MA 02148
(617) 322-3611
(FR) (CE)
CIRCLE 797

R. H. Carlson Co. Inc.
Norlabs Div.
41 Chestnut St.
Greenwich, CT 06830
(203) 531-5500
(CC) (EN) (EA) (PM) (RE)
CIRCLE 798

RTP Co.
580 E. Front St.
Winona, MN 55987-0439
(507) 4454-6900
(EL) (EP) (RE)
CIRCLE 799

Radstone Technology Corp.
20 Craig Rd.
Montvale, NJ 07645
(201) 393-2700
(MI)
CIRCLE 800

Ray Products Co. Inc.
11565 Federal Dr.
El Monte, CA 91734
(818) 579-4250
(CN) (CM) (EM) (IN) (ER)
CIRCLE 801

Raychem Corp.
Thermofit Div.
300 Constitution Dr.
Menlo Park, CA 94025
(800) 272-9243
(EM) (GP) (WT) (ER) (GK)
(TB) (EP)
CIRCLE 802

Resdel Corp.
Cape May County Ind. Park
Rio Grande, NJ 08242
(609) 886-1111
(EM) (GP) (TB)
CIRCLE 803

Richmond Static Control Services
870 Research Dr.
Palm Springs, CA 92262
(619) 325-3211
(ES) (ER)
CIRCLE 804

Richmond Technology Inc.
1897 Colton Ave.
Redlands, CA 92374
(909) 794-2111
(ES) (ER)
CIRCLE 805

Rittal Corp.
One Rittal Pl.
Springfield, OH 45504
(513) 399-0500
(BM) (CN) (CM) (EM) (GP)
(IN) (PT) (RA) (VR) (WT) (ER)
(VE) (WN)
CIRCLE 806

Robison Electronics Inc.
P.O. Box 8121
San Luis Obispo, CA
93403-8121
(805) 544-8000
(MP) (PM)
CIRCLE 807

Rogers Corp.
Microwave & Circuit
Materials
100 S. Roosevelt Ave.
Chandler, AZ 85226
(602) 961-1382
(CE) (FE) (LA)
CIRCLE 808

SIMCO
P.O. Box 1009
Miami, FL 33197
(305) 233-9900
(GP) (IN) (PT) (ER) (EP)
CIRCLE 809

SMI Ceramics America Inc.
2953 Bunker Hill Ln. #203
Santa Clara, CA 95054
(408) 982-0990
(MP) (ER) (CE)
CIRCLE 810

STRONGBOX
P.O. Box 2726
Culver City, CA 90231-2726
(310) 305-8288
(GP) (RA)
CIRCLE 811

Schlegel Corp.
Industrial Products Div.
1555 Jefferson Rd.
Rochester, NY 14623
(800) 828-6237
(ER) (GK)
CIRCLE 812

Schroff Inc.
170 Commerce Dr.
Warwick, RI 02886
(401) 732-3770
(BM) (EM) (GP) (IN) (PT) (RA)
(VR) (ER) (ER)
CIRCLE 813

Schurter Inc.
1016 Clegg Ct.
Petaluma, CA 94954
(707) 778-6311
(ER)
CIRCLE 814

Sescom Inc.
2100 Ward Dr.
Henderson, NV 89015-4249
(702) 565-3400
(BM) (CM) (GP) (IN) (RA)
(VR)
CIRCLE 815

Siecor Corp.
P.O. Box 489
Hickory, NC 28603-0489
(704) 327-5000
(CM) (RA) (VR) (WT)
CIRCLE 816

Southeastern Metal Products
1420 Metals Dr.
Charlotte, NC 28221
(704) 596-4017
(CM) (EM) (GP) (WT)
CIRCLE 817

Specialty Coating Systems Inc.
5707 W. Minnesota St.
Indianapolis, IN 46241
(800) 356-8260
(CC)
CIRCLE 818

Spira Mfg. Corp.
12721 Saticoy St. S.
North Hollywood, CA 91605
(818) 764-8222
(ER) (GK) (VE)
CIRCLE 819

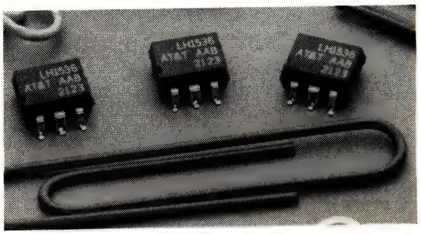
Stevens Products Inc.
128 N. Park St.
East Orange, NJ 07019
(201) 672-2140
(CM) (EM) (GP) (ER) (TB)
(EP) (LA) (PM)
CIRCLE 820

(see p. 169 for key)

(continued on p. 169)

▼ SOLID-STATE RELAY SUITS EUROPEAN TELECOM

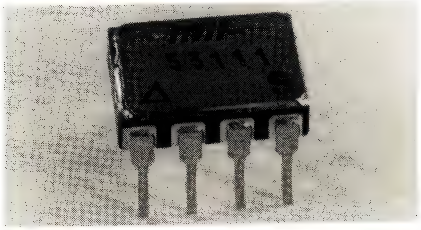
Exceptionally low on-resistance performance as required under European standards for parallel-phone applications is provided by the LH1536 1 Form B, high-voltage solid-state relay. The unit's typical on resistance is just 4 Ω with a current capability of up to 600 mA. In addition to general-purpose telecom applications, the relay is suited for industrial switching where low on resistance is specified. Input-to-output isolation is 3750 V ac and the part carries UL recognition as well as CSA and BABT certification. In lots of 10,000, pricing is $3.16. Packages are 6-pin DIP or gull-wing.



AT&T Microelectronics
Dept. AL-500404200
555 Union Blvd.
Allentown, PA 18103
(800) 372-2447, ext. 899
▶CIRCLE 671

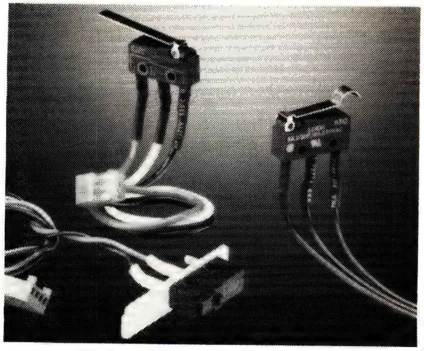
▼ MOSFET OPTOCOUPLER MIMICS SS RELAY

Maximum switching power in a miniature package is offered by the model 53111 power-MOSFET optocoupler, a fully hermetic device that operates as a solid-state relay. The unit comes in an 8-pin DIP and is guaranteed to operate over the temperature range of –55 to +125°C. Other features include a switching capacity of 0.8 A ac and 1.6 A dc; a low $R_{DS(ON)}$ specification; a 1500-V dc isolation test voltage; high transient immunity; and a 5-A output surge-current capability.



Micropac Industries Inc.
905 E. Walnut St.
Garland, TX 75040
(214) 272-3571
▶CIRCLE 672

▼ SNAP-ACTING SWITCHES PROVIDE FLEXIBILITY



A wide assortment of snap-in actuators and a variety of terminal styles including wire leads, connectors, and brackets gives the LC Series of subminiature snap-acting switches the flexibility to meet specific application needs. Available switch functions include SPDT, SPST-NO, and SPST-NC. Contact ratings are from low level to 10.1 A at 250 V ac. Electrical life is 100,000 cycles at 5 A and 250 V ac and mechanical life is 20 million cycles based on an operating force of 3.3 ozs. Prices start at $2.43 in lots of 500 with delivery from stock to six weeks.

C&K Components Inc.
57 Stanley Ave.
Watertown, MA 02172
(617) 926-6400
▶ CIRCLE 673

▼ PC-MOUNTABLE RELAYS TAKE WAVE SOLDERING

Epoxy sealing prepares the R25 Series of ac and dc relays for wave soldering and cleaning. The pcb-mountable devices are available with ratings of 10 and 16 A at 250/440 V ac and with either SPDT or DPDT contacts. They feature an upright package design and are immersion-proof. They're suited for a 5-mm grid pattern. Applications include heating controllers, servo motors, solenoid valves, and lifting magnets. Coil resistance is 280 Ω at 24 V ac and 5.6 kΩ at 120 V ac when using an ac power source, and ranges from 68 Ω at 5 or 6 V dc to 4.2 kΩ at 48 V dc when operated from dc. Call for pricing.

NTE Electronics Inc.
44 Farrand St.
Bloomfield, NJ 07003
(201) 748-5089
▶ CIRCLE 674

PACKAGING AND MATERIALS MANUFACTURERS

TRA-CON Inc.
Resin System Div.
55 North St.
Medford, MA 02155
(617) 391-5550
(ES) (ER) (EN) (EA) (PM) (RE) (SA)
CIRCLE 821

Taiyo America Inc.
1179 Fairview Dr., Suite E
Carson City, NV 89701
(702) 885-9959
(IK)
CIRCLE 822

Tech-Etch Inc.
45 Aldrin Rd.
Plymouth, MA 02360
(508) 747-0300
(ER) (GK) (SE) (VE) (WN)
CIRCLE 823

Techform Laboratories Inc.
Div. of Gardiner Metals Corp.
2021 N. Glassell St.
Orange, CA 92665
(714) 921-9054
(CC) (EN) (EA) (PM)
CIRCLE 824

Technit Inc.
129 Dermody St.
Cranford, NJ 07016
(908) 272-5500x234
(ER)
CIRCLE 825

Temp-Flex Cable Inc.
11 Depot St.
South Grafton, MA 01541
(508) 839-5987
(ER)
CIRCLE 826

Teradyne Inc.
Connection Systems Div.
44 Simon St.
Nashua, NH 03060
(603) 880-9461
(CM) (EM) (MI)
CIRCLE 827

The Carborundum Co.
Microelectronics Div.
10409 S. 50th Pl.
Phoenix, AZ 85044-5214
(602) 496-5000
(CE) (MC) (SU)
CIRCLE 828

Thermagon Inc.
3256 W. 25th St.
Cleveland, OH 44109-1668
(216) 741-7659
(EL) (EN) (EA) (LA) (PM) (SU)
CIRCLE 829

Thermofil Inc.
6150 Whitmore Lake Rd.
Farmington Hills, MI 48116
(810) 227-3500
(EP) (RE)
CIRCLE 830

Tracewell Enclosures Inc.
567 Enterprise Dr.
Westerville, OH 43081
(614) 846-6175
(BM) (CM) (EM) (GP) (IN) (PT) (RA) (VR) (ER)
CIRCLE 831

Transene Co. Inc.
Rte. 1 Tpke.
Rowley, MA 01969
(508) 948-2501
(CC) (EL) (EN) (EA) (PC) (PM)
CIRCLE 832

Triple E Corp.
The Foot of Crosby St.
Lowell, MA 01852
(508) 453-0600
(BM) (CM) (EM) (GP) (IN) (PT) (RA)
CIRCLE 833

Uniroyal Technology Corp.
Ensolite Div.
312 N. Hill St.
Mishawaka, IN 46544
(219) 256-8177
(GK)
CIRCLE 834

Uniroyal Technology Corp.
Uniroyal Adhesives & Sealants
312 N. Hill St.
Mishawaka, IN 46544
(219) 256-8655
(EA) (SA)
CIRCLE 835

Urban Chemical Co. Inc
151 S. Pfingsten Rd.
Deerfield, IL 60015
(708) 498-3080
(CC) (EA) (FL) (SO)
CIRCLE 836

Vector Electronic Co.
12460 Gladstone Ave.
Sylmar, CA 91342
(800) 423-5659
(BM) (CM) (EM) (GP) (IN) (PT)
CIRCLE 837

Vemaline Products
333 Strawberry Field Rd.
Warwick, RI 02887-6979
(401) 739-7600
(HS)
CIRCLE 838

Videojet Systems Int'l. Inc.
1500 Mittel Blvd.
Wood Dale, IL 60191-1073
(708) 860-7300
(IK)
CIRCLE 839

W. L. Gore & Associates
Electronic Prods. Div.
555 Papermill Rd.
Newark, DE 19711
(302) 738-4880
(ER) (GK) (SE) (VE) (LA) (SU) (TF)
CIRCLE 840

W. L. Gore & Associates
Electronics Prods. Div.
2401 Singerly Rd.
P.O. Box 1220
Elkton, MD 21922
(410) 398-6400
(ER) (GK) (SE) (VE)
CIRCLE 841

W. A. Miller Co. Inc.
Mingo Loop, P.O. Box 337
Oquossoc, ME 04964-0337
(800) 227-1415
(BM) (CM) (GP) (IN) (PT) (WT)
CIRCLE 842

Wilson Case Inc.
P.O. Box 1106
Hastings, NE 68902-1106
(800) 322-5493
(CM) (IN)
CIRCLE 843

Woodbine Industries Inc.
1574 Bridgewater Rd.
Bensalem, PA 19020
(215) 638-7600
(BM) (CN) (CM) (EM) (GP) (MI) (RA) (VR) (WT) (ES) (ER)
CIRCLE 844

Z Systems Inc.
3080 Olcott St., #110C
Santa Clara, CA 95054
(408) 980-1563
(MP) (SU)
CIRCLE 845

Zero-East
Zen Plastics
288 Main St.
Monson, MA 01057-0128
(413) 267-5561
(CM) (EM) (GP) (MI) (RA)
CIRCLE 846

Zippertubing Co.
P.O. Box 61129
Los Angeles, CA 90061
(310) 527-0488
(MI) (PT) (ER) (MG) (SE) (TB)
CIRCLE 847

Zymet Inc.
7 Great Meadow Ln.
East Hanover, NJ 07936
(201) 428-5245
(EN) (EA)
CIRCLE 848

KEY

Enclosures and Packages

(BM)	Bench mounted
(CN)	Consoles
(CM)	Custom design
(EM)	EMI/RFI design
(GP)	General purpose
(HS)	Heat sinks
(IN)	Instrument cases
(MP)	Microcircuit packages
(MI)	Military design
(PT)	Portable
(RA)	Racks
(VR)	Vertical racks
(WT)	Water tight

Materials

(CE)	Ceramics
(CC)	Conformal coatings
(EL)	Elastomers
(EN)	Encapsulants
(EP)	Engineering plastics
(EA)	Epoxies & adhesives
(PF)	Films, piezo
(FP)	Films, polyester
(FE)	Films, polyimide
(FL)	Fluxes
(IK)	Inks
(LA)	Laminates
(MM)	Magnetic materials
(MC)	Metal matrix composites
(MF)	Metalized fabrics
(PC)	Passivation coatings
(PM)	Potting materials
(RE)	Resins
(SA)	Seals
(SO)	Solders
(SM)	Solder masks
(SU)	Substrates
(TF)	Thick films

Shielding

(ES)	*Electrostatic*
(ER)	EMI/RFI
(FR)	*Ferrites*
(GK)	Gaskets
(MG)	Magnetic
(RC)	Rooms, chambers
(SE)	Sheets/strips
(TB)	Tubing
(VE)	Vents
(WN)	Windows

▼ LEAD-FREE SOLDER REPLACES LEADED TYPES

A lead-free solder is available for replacement of Sn63Pb37, Sn62Pb36Ag2, and Sn60Pb40 solders. Indalloy #227 takes their place with no required changes in equipment, process chemicals, or reflow profiles. The company's test results show that the solder compares favorably with common lead-based formulations in electrical and thermal conductivity, thermal coefficient of expansion, tensile strength, metalization compatibility, and wettability.

Indium Corp. of America
1676 Lincoln Ave.
Utica, NY 13502
(315) 853-4900
▶ CIRCLE 850

▼ THICK-FILM DIELECTRIC UPS MULTILAYER YIELDS

Multilayer circuits with high yields and high reliability result from use of Dielectric Composition H-100, which is part of DuPont's System H materials for gold multilayer interconnects. The thick-film dielectric features an average breakdown voltage of more than 1000 V/mil and is based on a crystallisable glass with a high softening point. A combination of fillers gives excellent resistance to oxygen-cell effects, and a close TCE match between the dielectric and the alumina substrate assures low levels of bowing. Call for pricing and delivery.

DuPont Co.
Barley Mill Plaza
Room G-52198
Wilmington, DE 19880-0010
(800) 237-4357
▶ CIRCLE 851

▼ ONE-COMPONENT EPOXY WITHSTANDS HIGH HEAT

A thermally conductive, one-component epoxy adhesive offers an operating temperature range of –100 to +400°F. The Supreme 10AOHT adhesive requires no mixing and is formulated to cure at elevated temperatures (1 hour at from 275 to 325°F). Tensile shear strengths in excess of 2500 psi and T-peel strengths of 30 pli are readily obtained. Application is without sagging or dripping even on vertical surfaces. The adhesive works well on metals, glass, ceramics, wood, vulcanized rubbers, and many plastics. Call for pricing and delivery.

Master Bond Inc.
154 Hobart St.
Hackensack, NJ 07601
(201) 343-8983
▶ CIRCLE 852

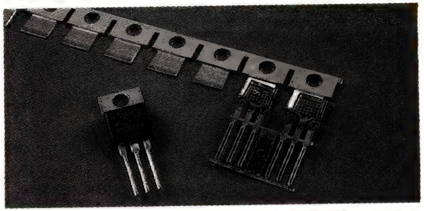
▼ FAN-SINK ASSEMBLY COOLS 486/586 CPUs

A fan-sink assembly that attaches quickly and securely to 80486 and Pentium microprocessors combats the growing problem of excessive heat build-up in systems. The Cool Snap fan sink controls the pressure between the heat sink and CPU, resulting in a secure, reliable fit that transfers heat quickly and efficiently. The design also eliminates the need to remove the chip from the pc board to install a cooling device. Many choices of height, numbers and styles of fins, and diameters up to 2-1/2 in. are available. Pricing is under $10 in lots of 100,000. Call for delivery information.

Vemaline Products Div.
Square Head Inc.
333 Strawberry Field Rd.
P.O. Box 6979
Warwick, RI 02887-6979
(800) 227-0254
▶ CIRCLE 853

▼ EPOXY ADHESIVE FILM CONDUCTS HEAT WELL

High thermal conductivity is featured in the T-gon 101 epoxy adhesive film. The material's thermal conductivity is 10 W/m-°C with thermal-resistance values of 0.06 to 0.10 °C-in.^{2}/W, depending on thickness. With its high dielectric strength of 500 V/mil and good adhesion, the film is not only capable of internally isolating TO-220 packages, but also of mounting components to substrates, lead frames to heat sinks, and pc boards to cold plates. Call for pricing and delivery.



Thermagon Inc.
3256 W. 25th St.
Cleveland, OH 44109-1668
(216) 741-7659
▶ CIRCLE 854

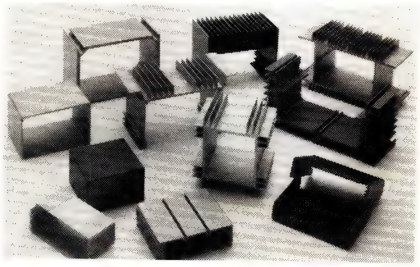
▼ SOLID THERMAL PLANES USHER HEAT AWAY

Available in SEM, VME, or custom configurations, a complete range of thermal-plane products cools circuitry in closed chassis without access to air. The products are of solid aluminum and offer five times the thermal conductivity of epoxy fiberglass/copper circuit boards. They're suited for designs where the thermal load is too much for the pc board itself, but not enough to justify active fluid cooling or exotic materials. Heat is removed from circuits and conducted directly to the chassis walls. Call for pricing and delivery information.

Lytron Inc.
55 Dragon Ct.
Woburn, MA 01801
(617) 933-7300
▶ CIRCLE 855

▼ EXTRUDED ENCLOSURES OFFER QUICK TURNS

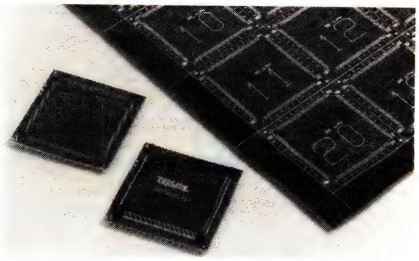
By using standard profiles, a line of more than two dozen extruded electronic enclosures can be designed, machined, finished, and delivered in less than two weeks. Custom enclosure profiles typically require about six weeks from design approval to delivery. If end plates or cover plates are required to complete an enclosure, the company has in-house tooling and stamping capability. As an example, model 660453B04000 is an anodized 3-by-1.787-by-4-in. hollow enclosure. Pricing is $2.67 in lots of 250.



Aavid Engineering Inc.
One Kool Path, Box 400
Laconia, NH 03247-0400
(603) 528-3400
▶ **CIRCLE 856**

▼ PLASTIC QFP ADAPTER SAVES BOARD DESIGNS

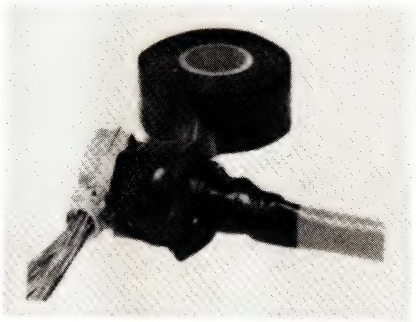
A 168- or 169-position plastic quad flat pack (PQFP) adapter allows cost-effective integration of PQFPs into pin-grid-array sockets. The adapter accommodates existing motherboard circuit designs and features a multilayer circuit board with 0.018-in. pins and alignment location features for easy surface mounting. The adapter allows use of less expensive PQFP devices instead of standard ceramic i486SX and DX PGA devices. Pricing for the PQFP adapter is $5 in lots of 5000.



AMP Inc.
P.O. Box 3608
Harrisburg, PA 17105-3608
(800) 522-6752
▶ **CIRCLE 858**

▼ MOLDABLE TAPES SEAL AND ENCAPSULATE

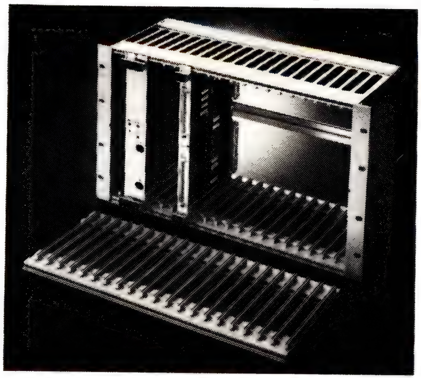
Developed as a replacement for heat-shrinkable tape, the Type TYT200 self-fusing silicone tape is well suited for molding, encapsulating, waterproofing, and insulating in applicaitons where a masking wrap or permanently resilient seal is required. The tape is self-adhering when wrapped under tension and fuses to form a homogenous mass within 24 hours at room temperature or 4 hours at 350°F. It won't crack or separate with thermal movement and is resistant to shock, vibration, weather, water, and ozone. Colors are black or red and the tape measures 1 in. wide by 0.020 in. thick. It comes packaged in 36-ft. rolls. Pricing in small lots is $17.85 per roll with delivery from stock to 4 weeks.



Cole-Flex
91 Cabot St.
West Babylon, NY 11704
(516) 249-6150
▶ **CIRCLE 857**

▼ EXTRUDED CARD CAGES INTEGRATES CARD GUIDES

A series of card guides integrated into a supporting panel is featured in an all-aluminum extruded card cage. The Triple E card cage's guide-and-panel combination is a one-piece aluminum extrusion that greatly increases the guides' strength and ensures easy insertion and removal of cards. The cage acts as a heat sink and, because the card guides are not plastic, the thermal path is uninterrupted. The guides also eliminate problems of flexing and breakage found with plastic guides. Cages are available to meet specs of all major bus architectures, including VMEbus, VXIbus, Multibus II, Futurebus, AT, and EISA. Call for pricing and delivery.



Triple E Corp.
The Foot of Crosby St.
Lowell, MA 01852
(508) 453-0600
▶ **CIRCLE 859**

▼ VMEbus ENCLOSURE BOASTS FLEXIBILITY

Stretching in any direction to meet various design criteria as well as accommodate peripherals, the Series L VMEbus enclosure comes in over 40 standard sleek, low-profile configurations. The units accept from one to five VME cards, a 110- or 200-W power supply, the company's card cage, and a Series TN eight-layer backplane that incorporates active automatic daisy chaining as well as dual fans. The units measure 1.9 in. high by 16 in. wide and 16.06 in. deep. Pricing starts at under $1000.

Electronic Solutions
6790 Flanders Dr.
San Diego, CA 92121
(619) 452-9333
▶ **CIRCLE 860**

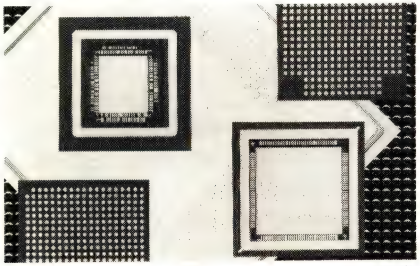
▼ HIGH AIR FLOW KEEPS ENCLOSURES COOL

Impeller blowers that provide over 100-lfm airflow across each slot are featured in Hybricon's line of high air-flow enclosures. The performance factor of blowers is greater than tubeaxial fans in the presence of the high back pressures common to many enclosure configurations. A wide range of standard designs ranges from 19-in. rack models to tower and desk-top configurations. Power supplies from 75 to 3000 W are available. Model R1021FA21SG3, which is 10U high by 21 in. deep, goes for $3750 in lots of one to four. Call for delivery.

Hybricon Corp.
12 Willow Rd.
Ayer, MA 01432
(508) 772-5422
▶ **CIRCLE 861**

▼ CERAMIC BGA PACKAGES OFFER HERMETICITY

Coors now offers the ability to convert its standard and custom ceramic pad-array carriers to ball-grid-array packages with the addition of solder balls after die attach. These cofired ceramics provide hermetic packaging with high electrical and thermal performance. The packages' high density, low cost per I/O, and assembly with standard surface-mount processes make them well suited for wire-bond, flip chip, and TAB devices. Call for pricing and delivery.



Coors Electronic Package Co.
511 Manufacturers Rd.
Chattanooga, TN 37405
(615) 755-5408
▶ CIRCLE 862

▼ SILICONE COMPOUND MEETS MIL STANDARDS

A source for silicones meeting MIL-A-46146B, Group II, Type I standards is found in Loctite's Product 5145 RTV silicone compounds. The non-corrosive, non-slumping, high-strength material is specifically formulated for bonding and sealing of electronic devices. When exposed to atmospheric moisture, the product cures to form a tough rubber sealant/adhesive for military, automotive, and industrial electronics. The cured elastomer resists weathering, moisture, and ozone degradation and retains flexibility from –65 to +400°F.

Loctite Corp.
705 N. Mountain Rd.
Newington, CT 06111
(203) 278-1280
▶ CIRCLE 863

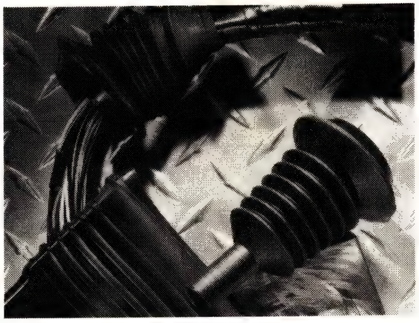
▼ SOLDER CREAMS ELIMINATE CLEANING

Using special rosin flux formulations, the Series 500ADV solder creams for surface-mount applications provide RMA activity. But after reflow, the slight flux residue is clear, hard, non-brittle, and remains stable and non-corrosive. The creams offer an environmental alternative to solvent cleaning or water washing and eliminate the cleaning step completely. The resulting solder joints are shiny, and the flux residue passes stringent surface insulation-resistance tests. A wide range of alloys, metal contents, and viscosities are offered.

ESP Inc.
14 Blackstone Valley Pl.
Lincoln, RI 02865-1145
(401) 333-3800
▶ CIRCLE 864

▼ MOLDED FEEDTHROUGH HEAT-SHRINKS TO FIT

A heat-shrinkable molded part is designed to seal and relieve stress on wire bundles in cable-to-bulkhead feedthrough locations. The feedthrough is made from a crosslinked, zero-halogen polyolefin material. Supplied in a highly expanded state, the feedthrough is easily and more quickly fitted over large, bulky connectors than conventional synthetic-rubber feedthroughs. The parts can be quickly shrunk down to a predetermined size to seal small-diameter cables as well. A variety of shapes is available to fit user needs. Call for pricing and delivery.



Raychem Corp.
300 Constitution Dr.
M/S 530/7568
Menlo Park, CA 94025
(800) 272-9243, ext. 1501
▶ CIRCLE 865

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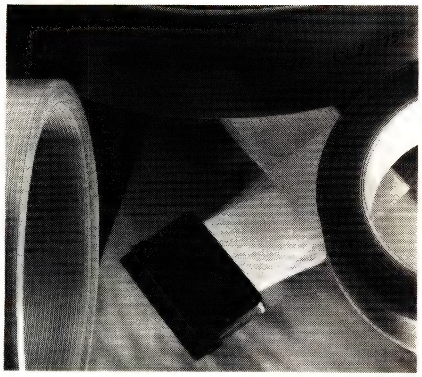
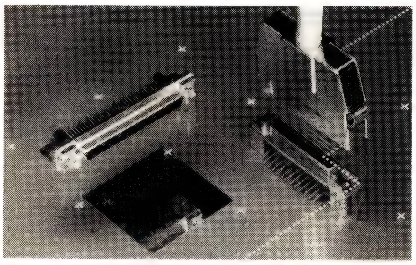
▼ TRANSMISSION CABLE MEETS SYSTEM NEEDS

A variety of transmission cables is offered with conductor sizes, impedances, and other electrical specifications that are matched to system requirements. The cables are well suited for high-speed and/or high-density signal buses in computer, automatic test, medical, telecommunication, and workstation applications. All cables feature silver-plated conductors and FEP insulation with a low dielectric constant of 2.0 to 2.2. Conductor pitches are as tight as 0.0125 in. in single-ended or differential signal configurations, and in shielded and jacketed designs. Pricing is from $0.01 to $0.05 per conductor foot depending on quantity and configuration. Delivery is in from four to eight weeks.



AMP Inc.
P.O. Box 3608
Harrisburg, PA 17105-3608
(800) 522-6752
▶CIRCLE 866

▼ SCSI-II CONNECTORS SPEED DATA TRANSFERS

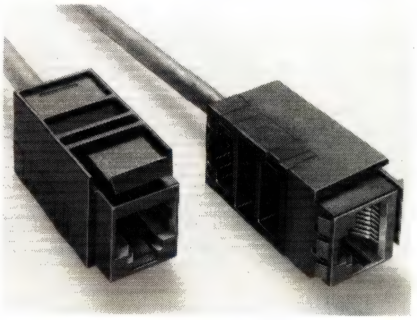


Engineered for fast, reliable data transfers, the Omega 9000 SCSI-II connectors boost the I/O performance of PCs and larger computers while facilitating their physical interconnection with peripherals. Featuring 0.050-by-0.100-in. contact spacing, the connectors come in 50- and 68-pin configurations as well as in cable-mount and vertical and right-angle styles. Their die-cast shells offer effective EMI/RFI shielding. These connectors conform to virtually all international standards for SCSI including those of ANSI, EIA RS-232, IPI-2, and HIPPI. In addition, they feature an easy squeeze-to-release latch mechanism for reliable cable-to-pc-board interconnections. Applications include small computers and peripherals, WORM drives, CD-ROMs, media-changer devices, scanners, optical-memory drives, and more. Call for pricing and delivery.

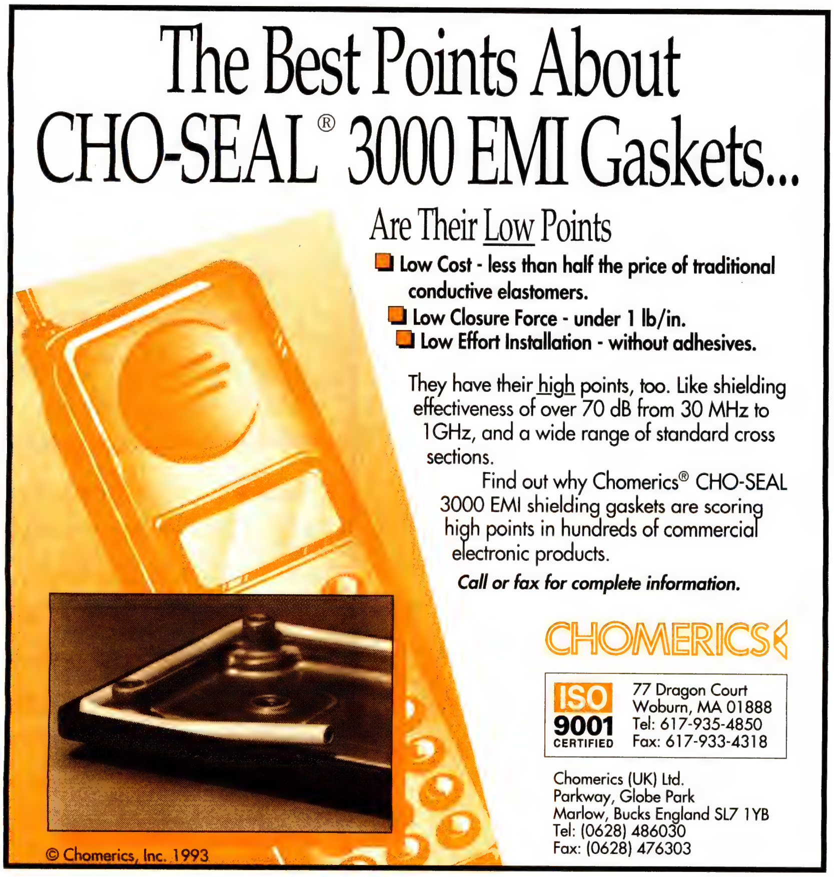
ERNI Components Inc.
520 Southlake Blvd.
Richmond, VA 23236
(804) 794-6367
▶CIRCLE 867

▼ CABLE-READY JACK STACKS SIDE-BY-SIDE

A narrow profile enables the Series SS 80 cable-ready jacks to be stacked side-by-side in space-restricted applications such as the front panel of a networking device. The jacks also feature the company's Load-and-Lace wire-management load bar for easy assembly. Wires from 26 AWG to 22 AWG, with maximum conductor diameters of 0.047 in., are usable. The jacks come in 8- and 10-contact configurations, have a snap-in panel mount, and are certifiable to FCC specifications with 50-μin. gold plating. Pricing is $2.50 in OEM quantities. Delivery is in from two to three weeks.



Stewart Connector Systems
RD 2, Old Trail
Glen Rock, PA 17327
(717) 235-7512
▶CIRCLE 868



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Chomerics (UK) Ltd.
Parkway, Globe Park
Marlow, Bucks England SL7 1YB
Tel: (0628) 486030
Fax: (0628) 476303

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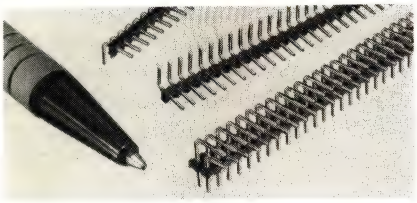
READER SERVICE 92

▼ 90° SQUARE-PIN HEADERS COME ON 2-MM SPACING

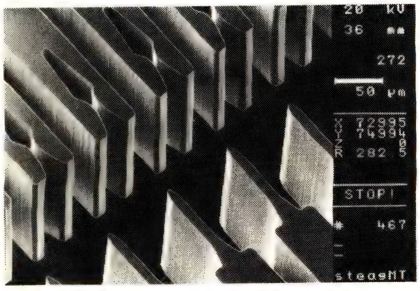
Added flexibility for making surface-mount or through-hole board-to-board connections, as well as for mating with Aries's 079 Series socket strips, is provided by the 2-mm Squarestix headers with 90° angle pins. The Series 29XX headers are offered in either a single-row configuration with from one to 50 pins, or in double rows with from two through 100 pins. Both versions come in SMT and through-hole styles. Users can also split the headers to any desired size and pin count. Pins are 0.020 in. square on 2-by-2-mm spacing. Pricing for a single-row header with 50 pins is $1.38 in lots of 10,000. Delivery is from stock to four weeks.



Aries Electronics Inc.
P.O. Box 130
Frenchtown, NJ 08825
(908) 996-6841
▶ CIRCLE 869

▼ CONNECTORS BOAST 80-μm CONTACT PITCH

The ability to manufacture multiple connector contacts at pitches as fine as 80 μm has been demonstrated, as have connectors with 130 pairs of gold-plated nickel contacts. The connectors are built on ceramic (aluminum oxide) substrates using ALC's strategic partner MicroParts's proprietary LIGA (from the German for lithography, electroforming, and plastic molding) microstructure technology. Integral macroscopic guiding elements ensure that the connectors are properly mated. Typical mating force is 1.5 cN (2.12×10^{-4} oz-force) per contact pair. Each pair of contacts carries 15 mA and has a resistance of 30 mΩ. Capacitance between adjacent contacts is 1.8 pF. The connector is not offered as a specific product but rather as a capability. Call for more information.



American Laubscher Corp.
80 Finn Ct.
Farmingdale, NY 11735
(516) 694-5900
▶ CIRCLE 870

▼ BACKPLANE CONNECTOR SPORTS METRIC GRID

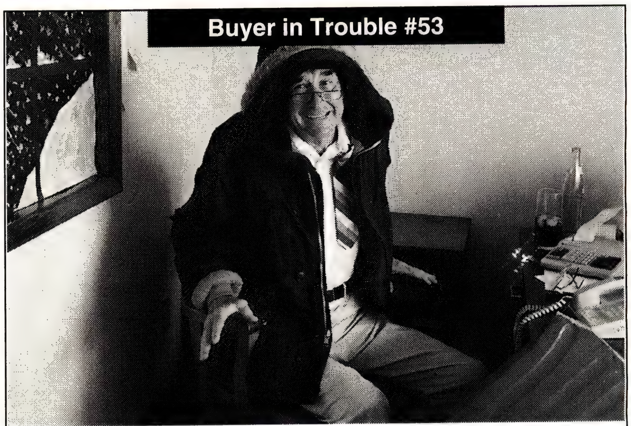
High contact density, a modular architecture, and Futurebus+ compatibility are all features of the High Density Metric (HDM) connector, a board-to-board backplane system based on the popular 2-mm metric grid. The connectors contain a six-row array of contacts. End-stackable signal, power, and polarizing/guidance modules can be arranged in virtually any configuration. Signal modules contain either 72 or 144 contacts, or 76 per linear inch. Two styles of daughterboard connectors are available: standard and shielded. Both versions mate with HDM backplane modules. Pricing in lots of 100 is $0.15 per pin.

Teradyne Connection Systems
44 Simon St.
Nashua, NH 03060
(603) 880-9461
▶ CIRCLE 871

▼ CUSTOM FLAT CABLES ARE EASY TO INSTALL

A film-bonding process results in made-to-order flat-cable systems in which a variety of individual wires are bonded to film carriers. This process enables engineers to specify a wide range of wire and cable insulation materials and construction types from Raychem's extensive line. Flexible and easy to install, the flat cables have applications in many wire-harnessing systems.

Raychem Corp.
300 Constitution Dr.
MS 530/7568
Menlo Park, CA 94025
(800) 272-9243, ext. 1501
▶ CIRCLE 872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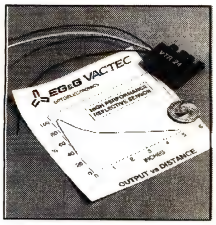
Prem Magnetics, Inc.
3521 North Chapel Hill Road, McHenry, IL 60050.
Phone: 815-385-2700. FAX: 815-385-8578.

READER SERVICE 136

▼ LONG RANGE SENSING IN MATCHBOX SIZE

Ideal for applications requiring object sensing and material control. The VTR24F1 retro-reflective optical switch extends the range of contactless, optical position sensing. Almost the size of a matchbox, it senses objects up to 4 inches. Designed to "see" almost any surface including matte, gloss, or black, this sensor provides a switchlike response, low position error, and CMOS compatibility.



EG&G Optoelectronics
Vactec Division
10900 Page, St. Louis, MO 63132
Phone (314) 423-4900
Fax: (314) 423-3956

READER SERVICE 195

▼ IR EMITTER AND DETECTOR CHIPS

Choose from an extensive line of photodiodes, photodiode arrays, phototransistors and IRED chips for OEM assembly applications. Photodiodes and photodiode arrays are available in both solderable and wire bondable configurations. Custom services are also offered.

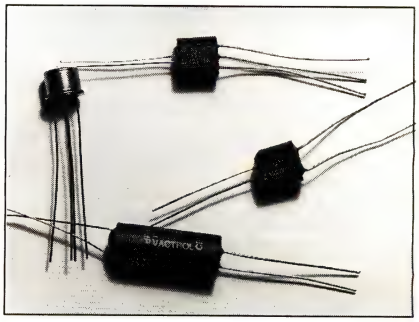
The IREDs are manufactured in 880 nm (GaAlAs) and 940 nm (GaAs) peak emission wavelengths using a state-of-the-art liquid phase epitaxial process which produces high power output and long operating lifetimes with a minimum of degradation.

EG&G Optoelectronics
Vactec Division
10900 Page, St. Louis, MO 63132
Phone (314) 423-4900
Fax: (314) 423-3956

READER SERVICE 196

▼ IDEAL FOR AUDIO APPLICATIONS

Analog Optoisolators (Vactrols™) are ideal as power limiters and remote gain control in audio amplifiers. Used widely in professional and automobile audio equipment, Vactrols™ provide low noise and low harmonic distortion making them ideal for use as electronically adjusted variable resistors. The Vactrols™ catalog discusses audio applications such as gating, muting, limiters, AGC distortion, and switching.



EG&G Optoelectronics
Vactec Division
10900 Page, St. Louis, MO 63132
Phone (314) 423-4900
Fax: (314) 423-3956

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▼ OPTIMIZED OPTICS

The VTE1285 high output IR Emitting Diode (IRED) incorporates an aspheric lens to optimize the amount of power focused into its output beam. This 5 mm diameter plastic package contains a 880 nm high efficiency IRED chip. Typical power output at 100 mA drive is 20 mW. Typical total half power beam angle is 16 degrees. A companion part, the VTE1295 is U.L. Component recognized. Applications include smoke detectors, remote controls, and security systems.

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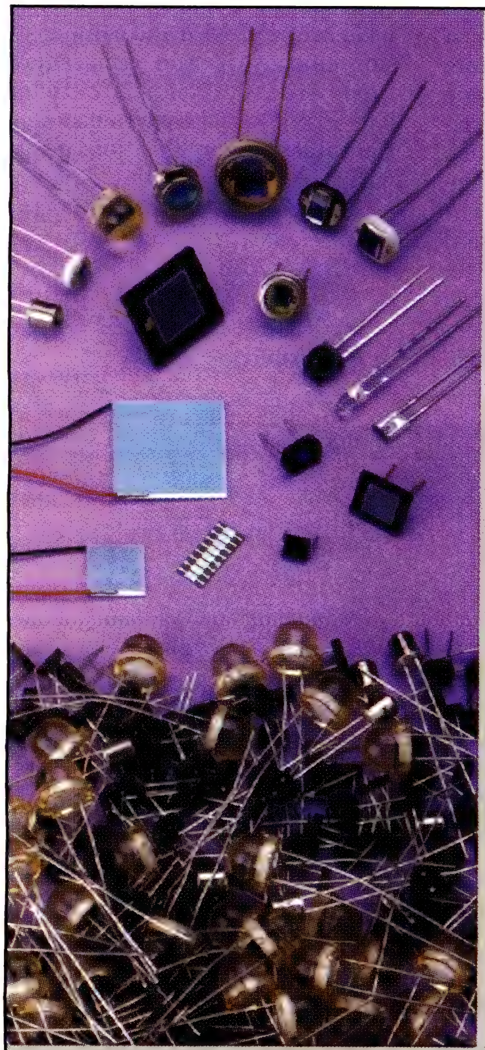

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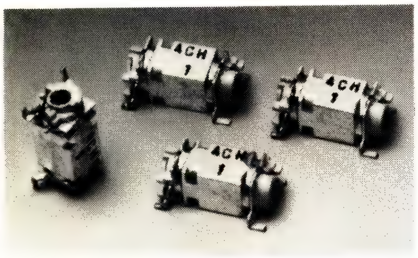
▼ SMT HELICAL FILTERS COVER 1.3 TO 2.5 GHz

Covering the frequency range of 1.3 to 2.5 GHz, the 4CHW Series of surface-mounted helical filters offers typical bandwidths ranging from 50 to 100 MHz. The devices provide a minimal footprint (9.5 by 5.8 mm), low profile (4.1 mm), and light weight, making them well suited for use with PCMCIA Type III cards.



Not only are the filters shielded to minimize packaging effects, but they're constructed so that the open end of the helical winding is placed inside the center of the filter, which eliminates any stray capacitance. Pricing starts at $8 in lots of 100. Tape-and-reel packaging is available. Call for delivery information.

Toko America Inc.
1250 Feehanville Dr.
Mt. Prospect, IL 60056-6023
(708) 297-0070
▶ **CIRCLE 875**

▼ TANTALUM CHIP CAPS SUIT PORTABLE TASKS

The TPS line of tantalum chip capacitors features low ESR values and high efficiency for use in power supplies for notebook computers, PDAs, PCMCIA drives, dc-dc converters, and cellular phones. Capacitance values range from 10 to 330 μF in EIA D and E case sizes. The parts are capable of higher ripple currents, lower ripple voltages, and less power and heat dissipation than competing devices. Call for pricing and delivery.

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Myrtle Beach, SC 29577
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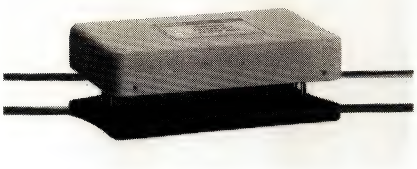
▶ **CIRCLE 876**

▼ OSCILLATOR PROVIDES TWO SIGNALS SANS PLL

A crystal oscillator that generates two precise timing signals at a constant 3:2 frequency ratio—without a phase-locked loop—is available from Bliley Electric. The Type NV9A Stratum III oscillator is oven-stabilized and voltage-controlled. Typical frequencies are 10.240 MHz and 32.768 MHz. Frequency stability is maintained within 1.5×10^{-7} from zero to 70°C. Frequency deviation is $\pm10\times10^{-6}$ at a control voltage of zero to +10 V. The units require power supplies of +15 V dc at 30 mA and +5 V dc at 1.3 A. Call for pricing and delivery.



Bliley Electric Co.
2545 W. Grandview Blvd.
P.O. Box 3428
Erie, PA 16508
(814) 838-3571
▶ **CIRCLE 877**

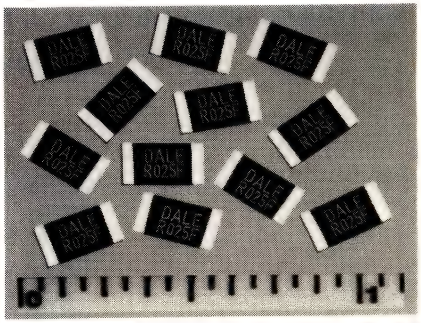
▼ SMT LED LAMP EMITS WHITE LIGHT

A surface-mounted LED lamp is being claimed as the first such device to emit white light. The WHITELED lamp features red, green, and blue light sources that can be illuminated separately, in pairs, or as a trio to create any color in the spectrum from yellow to purple. Applications include indicators used in the telecommunication, data-processing, industrial-control, or medical fields, or in any space-limited indicator application. The device is available for $2 in lots of 10,000. Small quantities are delivered from stock.

Siemens Components
Optoelectronics Div.
19000 Homestead Rd.
Cupertino, CA 95014
(408) 725-3508
▶ **CIRCLE 878**

▼ SMT CHIP RESISTORS PERFORM WELL FOR SIZE

By using a solid metal strip in place of a deposited metal-film element, Dale claims to have developed a new method for improving the performance-to-size ratio of chip resistors. The improvements to the WSL Series are represented by their combination of low resistance values, high stability, low inductance, and good power-handling characteristics in a standard chip footprint. Resistance values range from 0.01 Ω to 1 Ω in the 2512 (1-W) size. Applications include current sensing for battery monitoring in laptop PCs and a number of dc-dc-conversion circuits for handheld devices. Pricing for a 0.025-Ω, ±1% resistor is $0.38 in lots of 10,000. Delivery is in six weeks on tape and reel.



Dale Electronics Inc.
1122 23rd St.
Columbus, NE 68601-3647
(402) 563-6506
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A three-leaded, bicolor 5-mm LED indicator incorporates two GaP chips (red/green and yellow/green) and is able to produce three colors—red, green, and amber—as well as a range of colors in the spectrum between red and green. The Series 550-3x09 indicators are compatible with standard drive circuits. The red/green LED has an intensity of 5.0 mcd typical and forward voltages of 2.1 and 2.3 V typical. The yellow/green LED offers an intensity of 8.0 mcd typical and forward voltages of 2.1 and 2.1 V typical. Pricing starts at $0.96 in lots of 1000. Samples are available now with production quantities delivered in three to five weeks.

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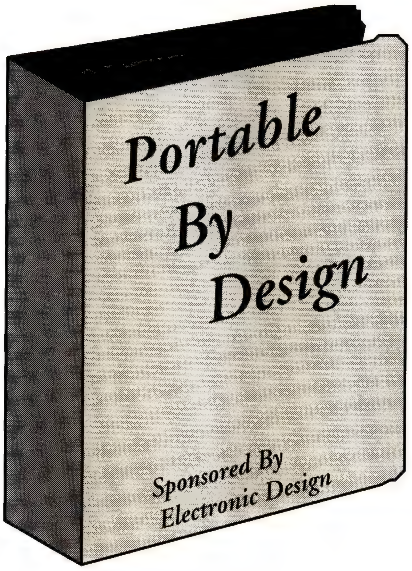

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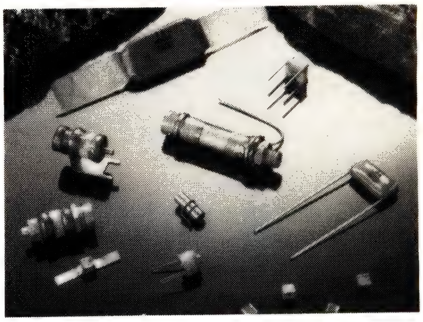

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Indianapolis, IN 46214
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Standard 1206 packaging enhances a line of multilayer ferrite-chip EMI suppressors by simplifying their use in production and improving board-space utilization. Model LCB-1206 offers 70-Ω at 100 MHz, while the ICB-1206 and JCB-1206 provide 90- and 150-Ω impedances at 100 MHz, respectively. All may be flow- or reflow-soldered. Video-graphics-board manufacturers will find particular use for the ICB-1206 suppressor because it enables their products to comply with FCC regulations without sacrificing clarity at the display's edges. Pricing for all three is $0.09 in lots of 100,000. Delivery is in six weeks.

Associated Components Technology
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CONTROLLER MANAGES POWER AND KEYBOARDS

AN 8-BIT MICROCONTROLLER TRIMS POWER DRAIN IN PORTABLE SYSTEMS BY MANAGING SUBSYSTEMS WITH FLASH-BASED PROGRAMS.

DAVE BURSKY

In the tight confines of portable electronic systems, space for the control electronics as well as the batteries to power the system is very limited. Consequently, components are usually soldered down, which makes it hard to upgrade systems if ROMs or EPROMs are employed to store the control programs. Furthermore, pc-board space is restricted, so multiple-chip solutions such as a microcontroller and separate decoder and memory chips might not be acceptable. Furthermore, to minimize battery size, intelligent power management should be included to dynamically control various subsystems, turning them on or off as needed. Finally, the man-machine interface—a keyboard, row of switches, or some other data-entry/output scheme—also must be managed.

By combining a large flash memory—32 kbytes—along with a power-management-smart microcontroller, designers at Hitachi came up with a second-generation chip that handles the keyboard to control the man-machine interface. The H8/3434 IKAP-II, which evolved from the company's H8/3332 and 3334 integrated keyboard and power management (IKAP-I) microcontrollers, provides an in-system reprogrammable/upgradable integrated solution to power and interface management. Despite its impressive capabilities, the keyboard-controller chip draws less then 5μA maximum in the standby mode *(see the figure)*.

In addition to the flash-memory-based version, another IKAP-II processor, the H8/3437, packs 60 kbytes of ROM space (either in mask-ROM or one-time programmable EPROM formats), giving designers lower-cost options for high-volume needs, or larger memory spaces to hold more complex control programs. Such large memory spaces will be needed to store next-generation complex keyboard BIOS firmware.

By moving power-management and man-machine control functions to a microcontroller, the host processor can be offloaded. Power management includes supervising battery charging and providing a battery-status indicator. Man-machine interface control covers the keyboards, mice, pens, and trackballs. Offloading the host (typically an 80486 or RISC processor) and moving the tasks to a lower-power processor—like an 8-bit microcontroller—means system power drains can actually be reduced. Such a simpler microcontroller, even with the additional keyboard control interface, would draw much less power than the host. The 3-V power-supply interface also helps minimize power drain, enabling the chip to meld into the portable system with little effort.

PROTOTYPE DEVELOPMENT

The on-chip flash storage of the H8/3434 provides an ideal medium for prototype development and fine-tuning of the control algorithms. Designers then can field systems and still easily update their internal control software. ROM or EPROM approaches would typically require removal of the memory or controller—and that means the chip would have to be socketed, which can be difficult if the chip has pin counts well above 68 leads. In addition, the socket may occupy too much space inside the equipment, making it unusable.

Thus, by using the flash, systems can be upgraded simply by downloading a new algorithm and rewriting the contents of the flash memory. Then, once the algorithms are tuned, ROM- or OTP-based versions of the controller can be substituted on the production line.

With its 10-MHz clock frequency and operating at 3 V, the register-based H8 architecture has plenty of throughput to handle power-management and interface-control tasks. In addition, the chip's highly integrated feature set gives the processor all of the resources it needs to monitor the system functions and battery, as well as control the subsystems. The host interface includes three Interrupt Request lines and the normal and high-speed gate A_{20} outputs for x86-based systems. Two byte-wide register sets help out on the host interface—data registers (for input and output) and a status register.

ABUNDANT FEATURES

Supporting the 8-bit processor core is a 1-kbyte RAM (the H8/3437 has 2 kbytes) that can hold a downloadable keyboard control matrix. In addition, an eight-channel 10-bit analog-to-digital converter provides high-accuracy resolution when sensing various system activities, such as battery-charge needs. A two-channel 8-bit digital-to-analog converter provides an analog output for backlight control and speech outputs.

The controller chip has 74 I/O pins, 16 for driving LEDs, eight for input only, and 48 with MOS input pull-up transistors. All of these features provide abundant control and output lines for all subsystem functions.

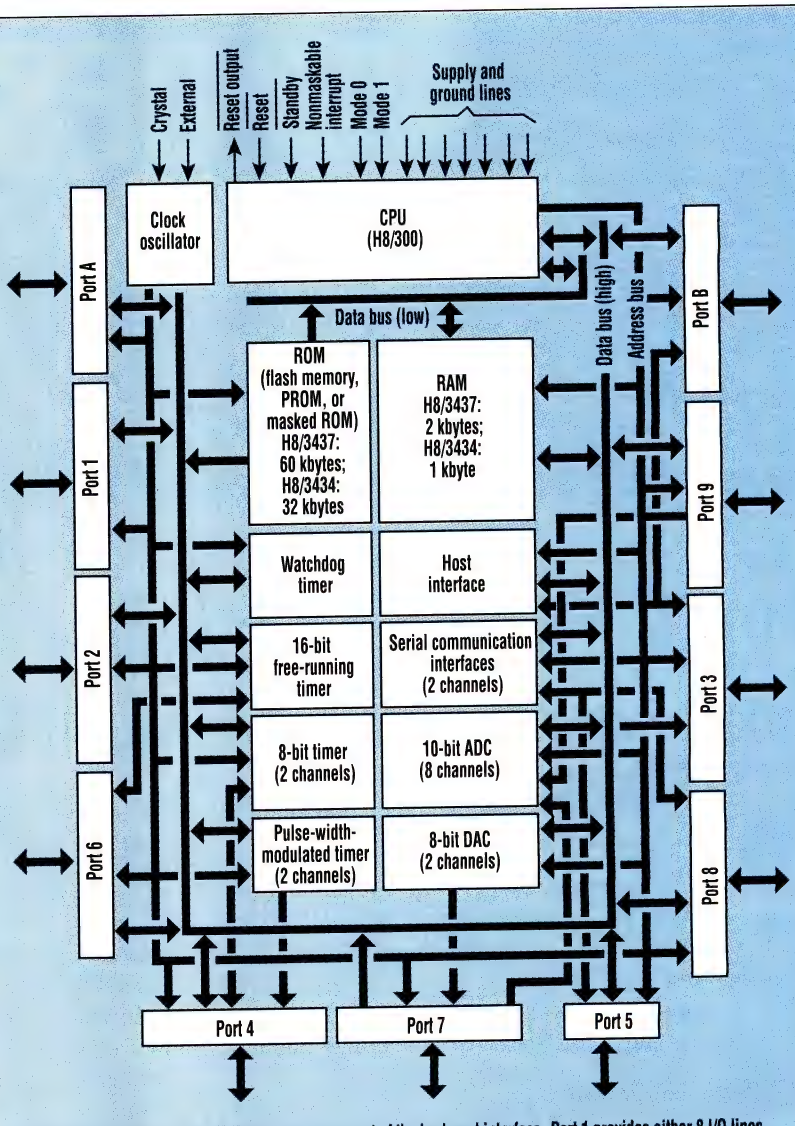
Two serial communication channels also are available. They can operate as either asynchronous or clocked synchronous ports and permit full-duplex communications. An on-chip baud-rate generator provides software-selectable clock rates for the serial ports.

Additional resources on the chip include two pulse-width-modulation timers, a pair of 8-bit timers, and one 16-bit timer to help control system activities. There's also a watchdog timer available to prevent program freezes/runaway.

To handle I/O functions, the controller chip incorporates an inter-IC (IIC) serial bus that implements the new industry-standard Access.bus interface for keyboard or other peripheral-I/O device attachment.

All told, the IKAP-II processors include all of the features of the IKAP-I chips plus 16 more I/O lines, and the ability to run at a clock frequency of 10 MHz with operating from just a 3-V power supply.

Alternatively, the processors can operate at a clock frequency of 16 MHz with a 5-V power supply. Being able to run at 5 V also lets the IKAP-II serve



Notes: Port A provides eight I/O lines or serves as part of the keyboard interface. Port 1 provides either 8 I/O lines or the lower half of the address, while port 2 provides 8 I/O lines or the upper 8 bits of the address. Port 6 provides either the rest of the keyboard control lines, or serves as an I/O port, or provides system control signals such as Interrupt Request lines and other signals. Port 4 provides either I/O lines, some Host Interrupt signal lines, and the timer input and output lines. Port 7 provides either the analog inputs for the ADC or the DAC outputs, or basic I/O functions. It ties the chip to the batteries and audio output device. Ports 5 and 8 include the serial I/O channels and part of the host-system interface, or can serve as standard I/O lines. Port 3 provides I/O lines, serves as part of the data bus, or becomes the interface to the host system databus. Port 9 either serves as I/O lines or provides many system control functions. And, port 8 either serves as I/O lines or as the other part of the host data-bus interface.

A COMPLETE SUBSYSTEM ON A CHIP aptly describes the highly-integrated IKAP-II processor designed by Hitachi. It includes a high-performance 8-bit processor core and 1 or 2 kbytes of RAM. Two versions are available: one with 32 kbytes of reprogrammable flash memory, and one with 60 kbytes of ROM or one-time programmable EPROM. A host of additional system resources for managing system power and the keyboard or I/O interface also are incorporated.

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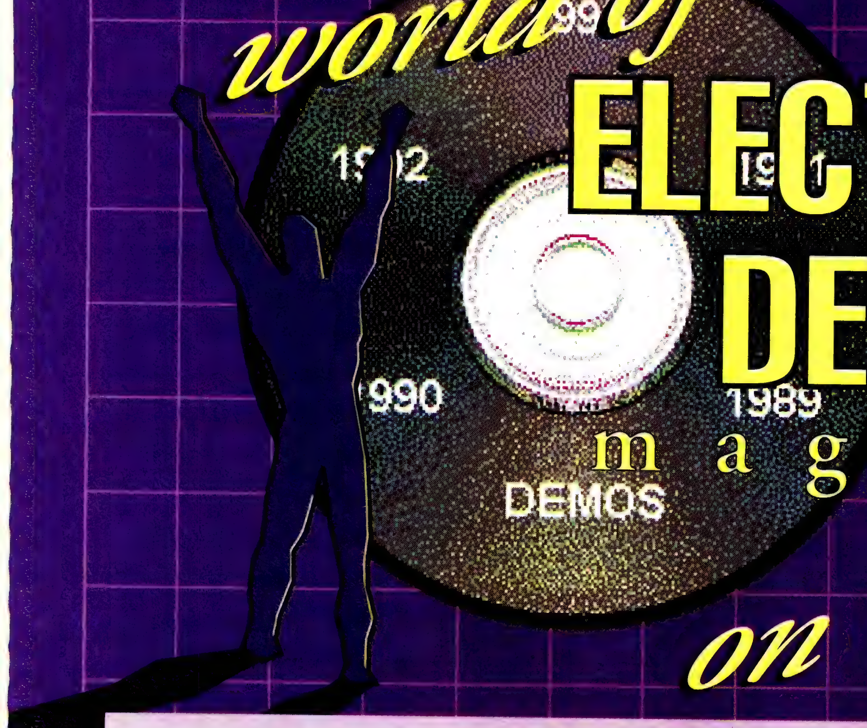

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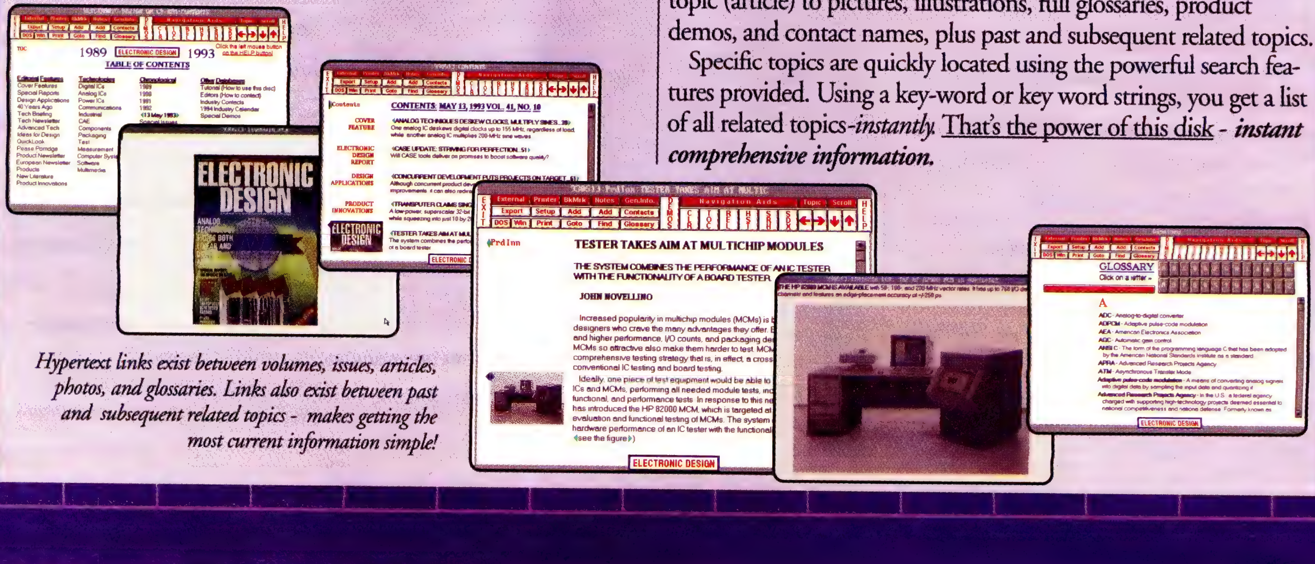
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TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER.

JOHN NOVELLINO

GLOSSARY
Click on a letter »

A
ADC - Analog-to-digital converter
ADPCM - Adaptive pulse-code modulation
AEA - American Electronics Association
AGC - Automatic gain control
ANSI C - The form of the programming language C that has been adopted by the American National Standards Institute as a standard
APRA - Advanced Research Projects Agency
ATM - Asynchronous Transfer Mode

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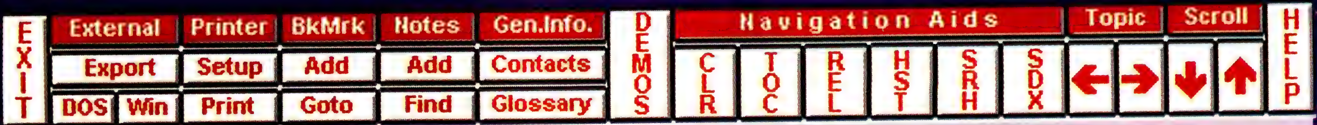

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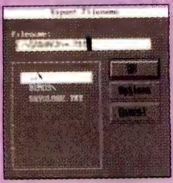

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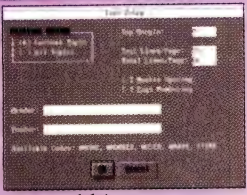

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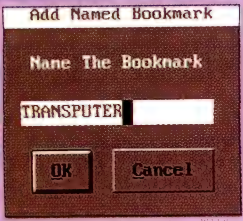

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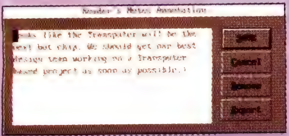

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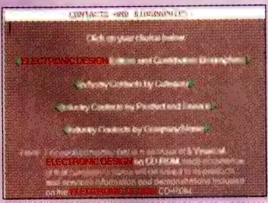

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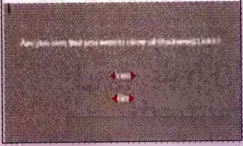

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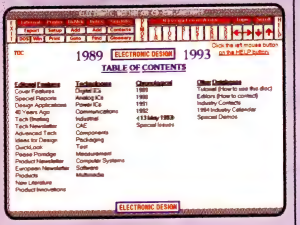

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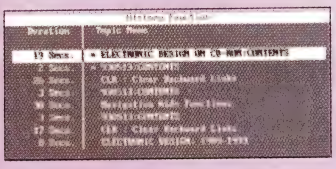

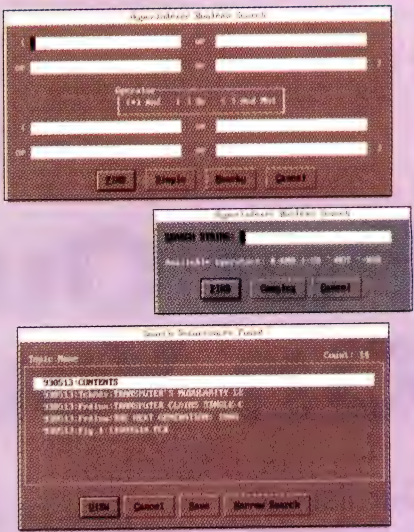

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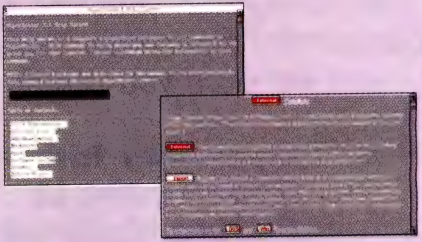

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in "green" desktop PC applications to manage the power of idle systems.

RECONFIGURABLE REGISTERS

The H8/300 core on the chip is a high-performance 8-bit controller with sixteen 8-bit general registers. These registers can also be reconfigured as eight 16-bit registers.

The CPU has an instruction cycle time of 125 ns, minimum, at a clock frequency of 16 MHz (an instruction cycle time of 200 ns at a clock frequency of 10 MHz), for an 8- or 16-bit register-register add operation. Instruction cycle time is 875 ns (at a clock frequency of 16 MHz) for an 8-by-8-bit multiplication operation.

The CPU has 57 basic instructions, including several powerful bit-manipulation operations. Instructions have a length of two or four bytes, which allows for single- or double-cycle loads for fast throughputs.

DEVELOPMENT TOOLS

Software development tools for the IKAP family are available from Hitachi and several third-party suppliers. Some of the tools include in-circuit emulators, C compilers, assemblers, linking editors, a librarian, and a simulator/debugger. Keyboard BIOS software for the older IKAP-I and the H8/3434 IKAP-II was developed by American Megatrends, Phoenix Technologies, and SystemSoft, as well as other vendors. These software packages implement most of the advanced features of the IKAPs, and can be purchased off-the-shelf or customized for a particular application. ☐

PRICE AND AVAILABILITY

The H8/3434 IKAP-II controller with 32 kbytes of flash memory and 1 kbyte of RAM comes in a 100-lead quad-sided flat package, and sells for $36 each in lots of 25,000 units. The H8/3437 version with 60 kbytes of OTP memory and 2 kbytes of RAM sells for $23.75 each in similar quantities. Lower-cost ROM versions also are available. Samples are available now, with mass production slated for late 1994.

Hitachi America Ltd., Semiconductor and IC Div., 2000 Sierra Point Pkwy., MS-080, Brisbane, CA 94005-1819; John Hull, (415) 589-8300. **CIRCLE 513**

HOW VALUABLE?	CIRCLE
HIGHLY	545
MODERATELY	546
SLIGHTLY	547

PRODUCTS NEWSLETTER

6-kW SUPPLIES FEATURE POWER-FACTOR CORRECTION

Using the latest power-supply technology and switch-mode techniques, the EA-9000 series laboratory supplies feature power-factor correction in units designed to output up to 6000 W. The three models—from Electro Automatic Corp., Lawrence, Mass.—were introduced at Electro '94. The supplies offer a high operating efficiency and a power factor of 0.98. Three versions are available: 0-18 V at up to 300 A, 0-36 V at up to 180 A, and 0-72 V at up to 90 A. Innovative design techniques result in low waveform distortion, interference, and weight. The units run on a three-phase, 185-to-265-V ac source. Unlike typical power supplies of this capacity, which require rack mounting, EA-9000 products are available in a benchtop configuration. Call Christine Strelow at (508) 687-6411. *JN*

CIRCLE 884

EDA ALLIANCE TO YIELD WINDOWS-BASED TOOLS

A strategic business alliance between Data I/O Corp., Redmond, Wash., and Intergraph Corp., Huntsville, Ala., promises to yield a comprehensive line of Windows-based EDA tools and expand product-distribution channels. In addition, the two companies will work with independent EDA developers to bring leading-edge tools to market. Many of the best new EDA tools come from small, independent developers who focus on a specific problem. Data I/O and Intergraph will cultivate these developers and bring their products to market, either as value-added components for existing applications, or as standalone products that can be promoted within the new distribution arrangement. Both companies are also working to embed knowledge of specific devices into their design products, helping to simplify the presentation of complex procedures. For details, call Data I/O at (206) 867-6852, or Intergraph at (205) 730-8532. *LM*

CIRCLE 885

ANALYSIS TOOL ENSURES PCB MANUFACTURABILITY

The Manufacturing Assurance Analyzer (MAA) from UniCAD Inc., Westford, Mass., is a tightly integrated data-collection and analysis environment that enables the sharing of manufacturability and design information. The analysis identifies problems and indicates possible solutions. Data is entered in the form of design stocklists; board technology; and component location, lead time, cost, and inventory. The tool analyzes the data and delivers a variety of reports. These reports may include manufacturing-cost analyses, production-equipment matching, manufacturing-plant suitability, and shared-assembly analyses. MAA is one of several pc-board tools from UniCAD, a new company formed to commercialize the EDA tools from Bell Northern Research Ltd. UniCAD will have a complete line of pc-board layout, analysis, and manufacturing tools. MAA runs on Unix workstations. It's available now for $12,000. Call (508) 692-8446. *LM*

CIRCLE 886

INFORMATION PUBLISHER EXPANDS DATA OPTIONS

A series of announcements from Information Handling Services (IHS), Englewood, Colo., expands engineers' option for obtaining and managing technical data. The company's Data and Application Integration Strategy (DAIS) gives engineers access to design data directly from their desktop software applications. This is an important capability for organizations that rely on a mix of internal data (corporate standards, product information, parts inventories) and external data from vendors, government agencies, and standards organizations. To pave the way for data and application integration, IHS has made both client and server enhancements to its existing 13-million-page technical-information services. On the client side, IHS enables users working in the MS-Windows environment to access and manipulate IHS data residing in CD-ROM format. On the server side, IHS has relational-database versions of three data libraries—Worldwide Standard Services, DOD Standardization Services, and the IC/Discrete Parametric Database. For each of these products, IHS will ship index and cross reference information in an Oracle database, along with IHS-developed SQL-based data-access tools. Users can access the IHS data through a menu-and-forms-driven interface that's consistent across Unix and PC platforms. The IHS Oracle products are available now. Also part of the DAIS initiative is the formation of a new services division dedicated to information an application integration. For more information, call IHS at (303) 790-0600. *LM*

CIRCLE 887

Edited by Clifford Meth

CALL FOR PAPERS

The Portable By Design Conference and Exposition

Sponsored by Electronic Design Magazine

Electronic Design is soliciting technical papers to be presented at the Portable By Design Conference February 15-17,1995 in the Santa Clara Convention Center, Santa Clara, Calif.

Engineers experience in designing portable electronic systems of all types are invited to share their expertise. The range of eligible design applications includes computing, communications, data-entry, navigation and instrumentation-in either vertical and horizontal markets.

Papers should emphasize problem solving and provide insights into specifying and designing portable systems.

General topics to be covered include: Microprocessors and microcontrollers;Power Sources and circuits;Power management techniques; Batteries; Connectivity(e.g. docking, public wired network and all wireless); Software(e.g. operating systems including proprietary OS and application development); Peripherals (e.g. PCMCIA, GPS, storage); Displays; Input devices; industrial, medical, and test equipment; and, System design considerations (e g accelerated product development, testing, size, ergonomics, packaging, and ruggedness)

To participate, respond to this call for papers by sending a one-paragraph abstract of a paper you would like to present. Papers should be oriented toward solving specific design problems.

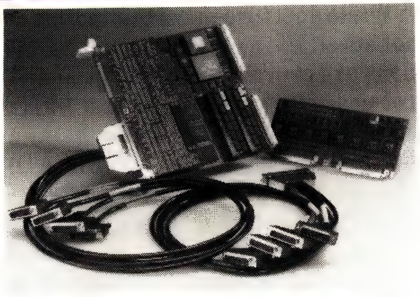
Abstracts should be sent to: *Program Chair, Portable By Design* Conference, c/o Electronic Design Magazine, P.O. Box 821, Hasbrouck Heights, NJ 07604. Or, send by fax to (201) 393-0204.

Deadlines:

Abstracts: October 10,1994

Full Papers: December 1,1994

COMMUNICATION MODULES CONNECT TO MULTIBUS II BASE BOARD



Two Modular Interface Extension (MIX) communication modules offer a higher throughput than their predecessors. The modules connect to a Multibus II base board. The MIX422 supports full-duplex sustained data rates greater than 38.4 kbaud and can sustain full-duplex T.1 data rates (1.544 Mbits/s) on selected channels. The MIX232 supports the RS-232 protocol and full-duplex sustained rates up to 38.4 kbaud.

The modules are designed for applications that require rapid data acquisition, such as telecommunications and industrial automation and control. The MIX422 is compatible with the RS-422 electrical specification and supports both the RS449 and X.21 physical layer communications protocols.

Both modules feature eight synchronous communication channels. Three modules can be stacked on the base board to increase the number of channels to 24. They can also be stacked with other modules to build multifunction I/O servers.

X.25 software drivers, which are a subset of Intel's iRMX III real-time operating system, will ship with the modules. Available now, the MIX422 and MIX232 communication modules each sell for $2695.

***Intel Corp.**, 2200 Mission College Blvd., Santa Clara, CA 95052; (800) 438-4769.* CIRCLE 890

■ *RICHARD NASS*

ISA CARRIER BOARD HOLDS 16 DSPS

One DON module holds four DSP3210 DSP chips and 64 Mbytes of DRAM in a space of about 10 sq. in. The TeraDON is an ISA bus carrier that has room for up to four DON modules. This supplies a peak performance of 533 MFLOPS. The board also features two Multi-Vendor Integration Protocol (MVIP) serial ports and an optional 200-Mbyte/s QuickRing interface. Software support for the board includes AT&T's VCOS real-time multitasking operating system and a comprehensive set of ready-to-run multimedia and telephony modules. Among these are fax, modem, text-to-speech conversion, speech recognition, and MPEG/P*64 audio compression.

Each module is connected to the AT bus through a shared 32-bit parallel interface, which is an extension of each module's 32-bit address-data bus. Each module can act as a bus master. Any DSP can interrupt the host. Conversely, the host can read or write to each module's RAM and control the reset and boot mode for each site. A TeraDON board with four DON modules sells for $9995 and is available now. A mechanical and electrical specification for the DON modules is also available.

***Ariel Corp.**, 433 River Rd., Highland Park, NJ 08904; (908) 249-2900.* CIRCLE 891

■ *RICHARD NASS*

CAPTURE, EDIT, AND PRESENT VIDEO ON A PC

The Videola Pro and Premium bring high-performance digital video down to the hands of the PC user. The cards come with bundled software to provide a complete video capture, editing, and presentation solution for Microsoft's Video for Windows. The only external connections needed to display full-motion video on the PC are a camcorder, VCR, or laser-disk player. Then the video can be played in any size window, even full screen. The video is captured on the hard disk in an Audio Video Interleaved (AVI) format. Full-motion video display is maintained during capture. This is useful in determining when to start and stop the capture process.

Using a feature called SuperZoom, video clips that have been stored on the hard drive using small windows can be played back on a full-screen window. Advanced scaling techniques help to maintain the high quality of the image. Any clips that are compressed in an AVI format can take advantage of the SuperZoom feature.

Video is compressed during the capture process on the Premium using the Motion JPEG algorithm to produce compression rations up to 50-to-1. The Pro offers a compression ration of about 3-to-1. The Videola Pro sells for $699 and the Premium costs $899.

***Orchid Technology**, 45365 Northport Loop W., Fremont CA 94538; (510) 683-0300.* CIRCLE 892

■ *RICHARD NASS*

ANTI-ALIASING FILTER SUPPORTS RUGGED APPS

Targeted for use in front of any analog-to-digital converter in military avionics, automotive, or other industrial data-acquisition system, the AAF-HE8P anti-aliasing filter is a rugged, RS-232 programmable low-pass filter. The eight-channel board features a 1-Hz-to-50-kHz software-selectable cutoff frequency range, dc accuracy, 0.5-degree phase matching between channels, and a five-pole Butterworth filter with a maximally flat pass-band and low-phase lag. Using an anti-aliasing filter with sharp attenuation eliminates the need to oversample the input signal. A fully configured AAF-HE8P anti-aliasing board sells for $3950 with large-quantity discounts available. RN

Alligator Technologies, 2900 Bristol St., Suite E-101, Costa Mesa, CA 92626; (714) 850-9984.

CIRCLE 893

12-BIT ADC SAMPLES AT 40 KHZ, RUNS OFF JUST 1 MA AT 3.3 V

When the venerable 574 12-bit ADC IC was announced over 15 years ago, few thought that they would one day see a sampling ADC with similar throughput rates—one that needed just 1 mA of current from a 3.3-V supply rail, or just 3.3 mW of power. But it has arrived in a tiny 24-lead SOIC package and sells for under $10 each in hundreds.

The HI5813, which uses CMOS switched-capacitor technology, is aimed at very low-power applications, such as cordless phones, DSP-based hearing aids, portable medical and test instruments, as well as PCMCIA Type II-based data acquisition pc boards and pen-based PCs. It will also find homes monitoring critical voltages in a variety of systems. Like most of today's general-purpose ADCs, the HI5853 employs a switched-capacitor successive-approximation architecture where signal sampling is inherent. Consequently, its 25/35-µs minimum conversion time (J/k-grade) includes the time to acquire the signal.

While aperture uncertainty time is not specified, ac (dynamic) specifications are provided, albeit typical and not near Nyquist. Sampling a 1-kHz input signal at 500 kHz results in a signal-to-noise distortion (SINAD) ratio of 63.9 dB for the J-grade device. The K-grade achieves a SINAD of 61.5 dB sampling 1 kHz at 600 kHz. Sampling similar signals at the same frequencies results in a total harmonic distortion (THD) of –71 dB for the K grade, 2 dB less for the J grade.

End-point integral and differential linearity errors over the extended industrial temperature range (–40°C to +85°C) run a maximum of ±4 LSB for the J-grade and ±2.5 LSB for the K-grade. The HI5813 is available in 24-pin plastic DIPs and SOICs and ceramic DIPs. In quantities of 100, the J-grade plastic DIPs go for $9.50 each, while the K-grade run just 95 cents more.

Harris Semiconductor Corp., P.O. Box 883, Melbourne, FL 32901; (800) 4-Harris, ext., 7199. **CIRCLE 894**

■ *FRANK GOODENOUGH*

HIGH-ENERGY EFFICIENCIES

A highly energy efficient family of 100-kHz pulse width modulating (PWM) switching regulators, the MIC2172/3172 are ideal for such applications as hand-held or portable equipment, where battery power preservation is critical. The MIC3172 version draws as little as 1 µA when shut down—a virtual 50-times improvement over previously released PWM switching regulators. With a 65-V, 1.25-A NPN power switch, the MIC2172/3172 supports all functions necessary to implement a step up/step down switching regulator. These devices are powered by as little as a 3-V supply, and as much as a 40-V supply, while drawing only 6 mA of current. Key features include frequency synchronization (MIC2172 model only), cycle-by-cycle current limiting, simplified loop stabilization, and fast response time to abrupt load current or input voltage changes.

Both the MIC2172 and the MIC3172 come in an 8-pin package with either a plastic mini DIP or SOIC format, operating in a temperature range of -40°C to +85°C. Also, an 8-pin package with a ceramic DIP format is offered, operating in a temperature range of -55°C to +125°C. All packages are available now in lots of 1000, and run about $2.25 each. CA

Micrel Semiconductor Inc., 1849 Fortune Dr., San Jose, CA, 95131; Marvin Vander Kooi, (408) 944-0800. **CIRCLE 895**

OFFER BUILT-IN PROTECTION

A family of ISOSMART IGBT power modules, the VIE 75-12S (75-A rating), VIE 100-12S (100-A rating), and the VIE 150-12S (150-A rating), can all operate at up to 20 kHz. The power modules were specially designed with a fully isolated gate drive, dual 1200-V, 150-A rated IGBTs connected as a half bridge with built-in protection for accidental short circuits. Each module has an on-board SMPS to power the gating and protection circuitry. They require only one, low-voltage, non-isolated power supply for a single-phase or multiple phase inverter. In addition, the modules are equipped with transformers to provide 2500-V input-to-output isolation, 15-V CMOS control inputs with Schmitt trigger characteristics, and an open-collector FAULT output pin. Both the power modules and their companion ultra-fast diodes offer low forward voltage drops and low reverse recovery currents. The VIE 150-12S, VIE 100-12S, and VIE 75-12S IGBT modules are available from stock. In lots of 10, they cost $228.15, $152.75, and $113.75 each, respectively. CA

IXYS Corp., 3540 Bassett St., Santa Clara, CA, 95054; (408) 982-0700. **CIRCLE 896**

TRANSISTOR FEATURES SMALL SIZE

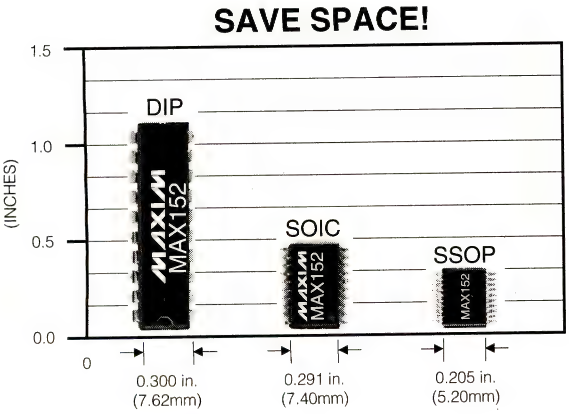
The MUN2111/2211, a series of bias resistor transistors, offer a simplified circuit design, board-space reduction, component-count reduction, and cost savings. It effectively replaces a single device design with its external resistor bias network. This is accomplished through one transistor containing a monolithic bias network, which consists of a series-base resistor, and a base-emitter resistor. Both resistors have a maximum collector voltage of 50-V dc. With a maximum collector current of 100 mA, the device has a maximum power dissipation of 200 mW. Both bias resistor transistors come in either NPN, designated MUN2211/2213, or PNP, designated MUN2111/2113, polarities. For low-power surface-mount applications, these devices are available in a SC-59 package, in either 8-mm tape or reel formats. Available from stock, the devices cost $0.12 each in lots of 3000 units. CA

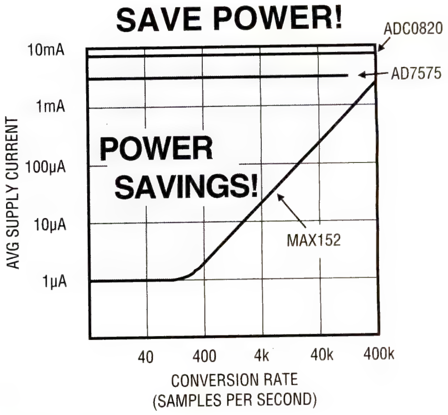
Motorola Inc., Semiconductor Products Sector, MD Z208, 5055 E. McDowell Rd., Phoenix, AZ, 85008; Dave Hollander, (602) 244-3742. **CIRCLE 897**

LOWEST POWER 3V ADC SHUTS DOWN TO 1μA

Ideal for Battery-Powered Systems!

Cut supply current to micro-amps in 3V systems with the new MAX152. It performs 8-bit conversions in 2μs, shuts down to 1μA between conversions, and powers up for the next conversion in 1μs.





- Single 3V Supply Operation
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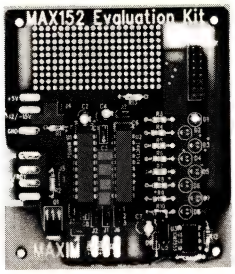
- 2μs Conversion Time
- Powerup in 1μs
- Low Price: $4.25*



Evaluation Kit Speeds Prototyping and Design

This pre-assembled kit provides a proven pc board layout and all parts needed to evaluate the MAX152 at up to 400ksps. Order MAX152EVKIT-DIP, $65†.

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PRECISION RAMDACs DELIVER SHARPER, HIGH-RESOLUTION IMAGES

DAVE BURSKY

Using a precision trimming scheme to keep the d-a converter output current to within 3% of its nominal value, the PrecisionDAC family of RAMDACs developed by AT&T Microelectronics delivers images that are sharper and more consistent than RAMDACs with equivalent resolutions. By keeping the current error to just 3%, the DAC outputs can control the image brightness accuracy to within 5%—an almost 250% improvement over most other available RAMDACs. The ATT20C and 21C families address workstation and high-performance PC-based graphics applications for desktop publishing, CAD, and many other areas that need high-resolution, high-uniformity displays.

To address the PC market, AT&T developed the 21C505/504, 20C506, and 20C510/511; for the workstation market, designers created the 20C565/57 and 568. All of the RAMDACs, though, support true-color graphics at resolutions ranging from 640-by-480 to 1600-by-1200 pixels. Multiple color display modes are supported by the three 256-byte on-chip lookup tables, or the tables can be bypassed for direct color inputs. The display modes include 8-bit pseudo-color, 15/16-bit high color, and 24-bit true color.

The highly integrated chips include precision voltage references, clock synthesizers and precision PLL-based analog clock multipliers, simplifying overall system design and eliminating the need to route high-frequency pixel clocks on the circuit board. By integrating the reference on the chip, the reference can be trimmed during the manufacturing process, thus delivering a "pre-tuned" RAMDAC to the system designer.

The analog clock multipliers included on the chips provide substantial benefits versus the digital clock doublers most other companies have used—digital doublers typically provide non-symmetrical duty cycles in the pixel clock, therefore output pixels have inconsistent widths. That results in inconsistent gray-scale images because such images consist of adjacent (and thus different width) black-and-white pixels.

Also included in the RAMDACs is a new pixel format with embedded visual control bits, which simplify software schemes that want to switch display modes on-the-fly. Furthermore, the RAMDACs were built with "green" systems in mind—they have three ways to address power reduction for Energy Star compliance. First, the design of the RAMDACs was done to keep active power to a minimum, with mid-range family members consuming about 1.5 W, and high-end members consuming about 1.8 W.

Second, all the RAMDACs support power-management schemes, and under software control can be placed in one of four reduced-power modes. Third, the deepest sleep modes trim the current drain to just 3 mA, yet allow the color look-up tables to retain their color maps.

The 21C505 and 504, 20C506, and 20C510/511 offer 32 to 64-bit pixel ports and hardware cursor support, an overscan RAM for border colors, and a dedicated 8-bit super VGA port. The chips come in 135-, 150-, and 170-MHz speed grades. Depending on the model, the number of display modes ranges from a low of about 10 up to 38 in the high-end units. Some of the modes include 24-bit true color, and multiplexed pixel formats ranging from 32 1-bit (monochrome) pixels on the 21C505/504 to two 16-bit pixels on all family members. The 20C506 and 511 also support a packed-pixel format, in which four (20C506) or 8 (20C511) 24-bit pixels can be loaded into the RAMDAC during three consecutive frame buffer data-output cycles. That permits the graphics system to support higher true-color resolution without requiring a faster frame buffer.

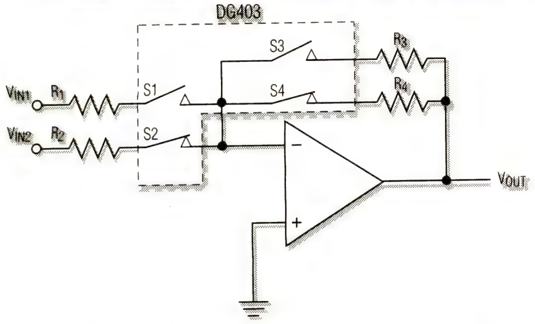
The entry-level version, the 21C504, has speed grades of 85 and 110 MHz, a 32-bit pixel port, a 32-by-32-by-2 cursor memory, and requires direct frequency inputs (no clock doubler on chip). The mid-range 20C505 doubles the cursor memory and adds the PLL-based clock doubler. Adding dual clock synthesizers, a packed 24-bit pixel mode, double buffering on the data path, the 20C506 can take on the workstation and high-end PC applications. Tak-

(continued on page 194)

IMPROVED DG400 SERIES GUARANTEES 3Ω *MATCHING* & 4Ω *R_{ON} FLATNESS* FOR FREE!

The Only DG400s with Guaranteed Charge Injection

PROGRAMMABLE GAIN AMPLIFIER



Switching into a virtual ground reduces distortion caused by $r_{DS(ON)}$ variation over the analog signal range. Guaranteed $r_{DS(ON)}$ matching (typically 0.5Ω) ensures gain accuracy of <0.01% when R1 through R4 are greater than 10kΩ.

Maxim's new, improved DG400 series of switches are upgrades to industry-standard DG400 devices. These devices meet all original DG400 specifications. Their tested parameters for RON matching and flatness have never before been guaranteed. These new specifications assure lower distortion and improved linearity and accuracy for attenuators, tuned filters, sample and hold, and programmable-gain amplifiers. All switches operate over a wide supply voltage range of 10V to 30V or ±4.5V to ±20V.

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IMPROVED PRODUCT	R_{ON} MATCH (Ω)	R_{ON} FLATNESS (Ω)	Q_j (pC)	OFF LEAKAGE at +85°C (nA)	ON LEAKAGE at +85°C (nA)
DG401/3/5	2	3	15	5	10
DG411/2/3	3	4	10	5	10
DG417/8/9	3	4	10	5	10
DG421/3/5	3	4	10	5	10
DG441/2/4/5	3	9	10	5	10

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(continued from page 192)

ing aim at portable systems, the 20C510 will double the size of the pixel port to 64 bits and provide an interface for a flat-panel display. Lastly, the 20C511 is like the 510, but it drives CRTs and adds a double-buffered 64-bit pixel port to the feature list.

Supporting the high-end workstation applications, the 20C565, 567, and 568 offer 47 display modes, provide 64-bit pixel ports, and include 4-by-24-bit overlay RAM arrays that can be used to set border and background colors. The chips are available in 135- and 170-MHz speed grades and support double frame-buffer designs, which permit boards to offer clean image outputs during time-consuming 3D graphics rendering and shading operations. Three clock synthesizers on the 20C565 and 568 produce synchronous system and shift clock outputs and a load-clock multiplier, which eliminates the need for a separate pixel clock. The 20C567 and 568 also contain three 256-word-by-8-bit ROM-based color lookup tables for dedicated gamma correction. The ROMs are programmed during chip manufacturing to optimize the RAMDAC for a specific monitor.

The RAMDACs include a new feature that allows the host graphic controller to switch, on-the-fly, among the RAMDAC display modes on a pixel-by-pixel basis. The RAMDACs allow the graphics controller to store visual control bits in the frame buffer alongside standard RGB pixel data. The controller can then use these bits, for example, to swap between color-RAM and color-RAM-bypass display modes, and to control double-buffer operations.

Samples of some of the Precision-DAC family of RAMDACs are immediately available, while the remaining units will be sampled later this year. In lots of 10,000 units, prices are as follows: $11 for the 21C505, $14.50 for the 21C506, $23 for the 21C510/511/565, and $32 for the 21C567/568.

AT&T Microelectronics, Dept. AL-500404200, 555 Union Blvd., Allentown, PA 18103; (800) 372-2447, Dept. P11 (in U.S.); (610) 778-4106 (fax requests). **CIRCLE 898**

16-BIT MICROCONTROLLER ADDS DUAL-MODE SYSTEM BUS

The established MCS 96 family of advanced 16-bit microcontrollers has gained a new member, the 8xC19NP. The Intel microcontroller, aimed at embedded applications, supplies a dynamic dual-mode system bus with a MUX-DEMUX and a chip-select unit. The demultiplexed bus allows the use of lower-cost memory, thereby reducing the total system cost. An additional savings is achieved because the chip-select unit requires no glue logic. This reduces the overall board space, as well.

The 8xC196NP comes with a 1-Mbyte linear address space to reduce access time and eliminate the complexity of banked memory designs. It also has a 1-kbyte register RAM and 4 kbytes of on-chip ROM. The integrated four-channel Event-Processor Array module is used for high-speed event monitoring and generation.

The controller can run at either 25 MHz at 5 V or 16 MHz at 3.3 V, making the device suitable for portable applications. A host of development tools are available to support the chip, including ApBuilder, a Windows-based tool that acts as a learning and reference guide and an application builder for embedded-control applications.

The 8xC196NP 16-bit microcontroller is now sampling. Production volumes will be available in July. The part is housed in a 100-lead quad flat-pack (QFP) or a shrink quad flat pack (SQFP). The ROMless versions sells for $16.50 for the QFP, and $17.40 for the SQFP, both in quantities of 100. With the ROM, the parts rise to $19.50 and $20.60, respectively. For more information, request document # 272469-001 from Intel.

Intel Literature Center. *P.O. Box 7641, Mt. Prospect, IL 60056; (800) 548-4725.* **CIRCLE 899**

■ *RICHARD NASS*

PIPELINED BURST SRAM SPEEDS CACHE SUBSYSTEMS

By adding pipelining and a synchronous interface to its high-speed static memories, designers at Samsung have crafted a high-speed memory ideal for the highest-performance Intel Pentium CPUs, as well as RISC processors. With the ability to run in systems with clock speeds of up to 75 MHz, the synchronous, pipelined, burst SRAMs also operate from a 3.3-V supply, thus suiting them well for use in the CPU "cluster" (the CPU, cache controller and cache memory) which, with most of the latest CPUs, requires a 3.3-V supply.

The KM732V588 and KM732V592 are 1-Mbit memories, both organized as 32 kwords by 32 bits. They operate with a two-stage data-and-address pipeline to minimize memory access delays. The KM732V588 is optimized for the Pentium's interleaved burst mode, while the KM732V592 has a linear-address-burst mode. All data, address, and control inputs are sampled and all outputs are valid on the positive-going edge of the system clock. Such an arrangement simplifies system designs and gives designers better control over their memory system.

The internal data, address, and control latches and on-chip burst address generator and high-output-drive circuits eliminate many of the support chips required in previous high-performance systems, thus simplifying the system and reducing the board area needed for the cache.

The synchronous SRAMs will be sampled late this summer and will sell for $22 each for the 50-, 60-, or 66-MHz versions. Production quantities will be ready in the first quarter of 1995.

Samsung Semiconductor Inc., *3655 North First St., San Jose, CA 95134-1708; (408) 954-7000.* **CIRCLE 900**

■ *DAVE BURSKY*

I_{DDQ} TOOL MANAGES POWER, ADDS CONTROLLABILITY

As a tool for I_{DDQ} test development, Current Synthesis automatically synthesizes and places test logic structures on cell library-based ICs. The new software, an enhancement module for CrossCheck's CurrenTest I_{DDQ} product, improves chip power management by eliminating current-draining conditions and reduces vector count and test time.

By improving the quality of the functional vectors used by CurrenTest, Current Synthesis significantly reduces the number of vectors needed for high fault coverage. To improve power management for I_{DDQ} testing of both synchronous and asynchronous circuits, the module eliminates bus contentions and floating buses by synthesizing structures, such as control gates and bus keepers. Also, current-draining cells, such as sense amplifiers for RAMs, analog comparators, and band-gap references, are modified with synthesis structures to reduce current. The result is higher test reliability, longer battery life in portable applications, and a lower pass/fail current limit.

The module disables ring oscillators during I_{DDQ} measurements to improve current sensing during testing. In addition, Current Synthesis improves controllability of deeply embedded logic nodes that are difficult to toggle. Various test logic structures, such as multiplexers and other nonscan control logic gates, are synthesized automatically, which makes it easier for test-pattern-generation tools to create higher defect coverage.

Current Synthesis comes as an add-on module to CurrenTest, starting at $15,000 per seat, depending on packaging and options. First shipments will begin in the third quarter, with full production shipments scheduled for the fourth quarter. CurrenTest starts at $45,000.

CrossCheck Technology Inc.,
2833 Junction Ave., Suite 100,
San Jose, CA 95134; (408) 432-9200. CIRCLE 902

■ *JOHN NOVELLINO*

COMPACT DATA-ACQUISITION SYSTEM INCLUDES EXPANSION SLOT

The DaqBook/112 is a 12-bit, 100-kHz data-acquisition system with a built-in expansion slot, all in an 8.5-by-11-by-1.375-in. package designed to fit under a notebook PC. The unit offers eight differential or 16 single-ended analog inputs, two 12-bit analog outputs, four digital inputs, four digital outputs, and one counter-timer.

Shipped with the DaqBook/112 is DaqView2, a Windows-based data-acquisition software package that allows users to set up their applications, view data in real time, save acquired data directly to disk, or seamlessly transmit it to other Windows applications, such as spreadsheets and data bases. The software requires no programming skills and supplies thermocouple linearization and cold-junction compensation.

The DaqBook connects directly to a notebook PC's enhanced parallel port, which permits 700-kbyte/s bidirectional data transfers. The unit can also be connected through a standard parallel port and has a pass-through feature that allows simultaneous connection to a parallel printer. An optional PCMCIA interface card permits connection through a PC's PCMCIA card slot.

A number of signal-conditioning cards support the DaqBook/112. Two new cards include the DBK17, a four-channel simultaneous sample-and-hold card that allows multiple channels to be sampled within 50 ns of one another. Also, the DBK18 provides four low-pass filters that can be individually configured for cutoffs from dc to 50 kHz and for Butterworth, Chebychev, or Bessel characteristics.

An ac adapter is included with the DaqBook/112, and it can also be powered by a car battery or any 7-to-30-V dc source. An optional rechargeable battery module supplies up to 6 hours of operation.

The DaqBook/112 costs $1295. The DBK17 sample-and-hold card and DBK18 low-pass-filter card each cost $495. The DBK35 PCMCIA interface card and cable cost $195. Delivery is in two weeks.

IOtech Inc., *25971 Cannon Rd.,*
Cleveland, OH 44146; (216) 439-4091. CIRCLE 903

■ *JOHN NOVELLINO*

RF COUNTER MAKES FAST, EASY MEASUREMENTS

The HP 53181A RF counter makes fast, high-resolution measurements and features an intuitive user interface that simplifies operation. The unit offers 10 digits of resolution per second, with a digit-blanking function that eliminates unneeded digits for faster reading of the display. Basic measurements are made with one button push, and a self-guided, shallow menu tree allows access to other commonly used functions. Bandwidth is 225 MHz. Second channel options provide either 1.5- or 3-GHz coverage. An automatic limit-testing function has an analog display mode that visually shows whether a measurement is within limits. Other features include built-in statistics and math functions, an IEEE-488 port, RS-232 printer support, and a data-transfer rate of more than 200 fully formatted measurements per second. The HP 53181A costs $1500. The 1.5-GHz second channel is $500, and the 3-GHz second channel, $800. Delivery is in two weeks. JN

Hewlett-Packard Co., Direct Marketing Org., P. O. Box 58059, MS51L-SJ, Santa Clara, CA 95051-8059; (800) 452-4844, ext. 8327. CIRCLE 904

IC TESTER FAMILY COVERS MULTIPLE APPLICATIONS

With the addition of four models, the HP 83000 family of digital-IC testers covers a wide performance range in both engineering and production environments. The HP 83000 F330i and F240i supply data rates to 330 and 240 MHz, respectively, for engineering uses such as prototype evaluation and analysis of production rejects. The F120t and F80t, with maximum operating frequencies of 120 and 80 MHz, respectively, are optimized for high throughput in production use.

The F240i and F330i feature a test processor per pin on up to 512 channels, with full timing, waveform, and error analysis capability on each pin. They incorporate an integral test head. The F80t and F120t are full-blown production testers with a specially designed external test head manipulator, as well as fast design-to-test links and short setup times. Their overall timing accuracy is ±300 ps and maximum channel count is 512. All the systems are prepared for eventual expansion to 1024 channels.

Other features include "on-the-fly" waveform changes, which allow users to compose complex timing patterns, and programmable loads, which create a truer representation of real-world operation. The systems have a graphical user interface in a Windows environment. Device characterization is aided by overlay schmoo, softscope, waveform edit, and error mapping capability.

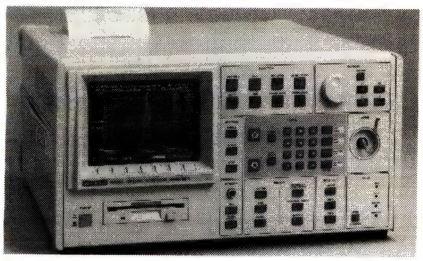
Prices vary according to configuration. For 256-channel systems, approximate per channel prices are: $4500 for the F330i, $3300 for the F240i, $4100 for the F80t, and $4900 for the F120t. The F330i and F240i will be available for order in July, with first shipments in September and October, respectively. The F80t and F120t can be ordered now, for first shipments in September and November, respectively.

Hewlett-Packard Co., *Direct Marketing Org., P. O. Box 58059, MS51L-SJ, Santa Clara, CA 95051-8059; (800) 452-4844 ext 8167.* **CIRCLE 905**

■ *JOHN NOVELLINO*

OPTICAL ANALYZER HAS WIDE DYNAMIC RANGE

The Advantest Q8383 optical spectrum analyzer features a dynamic range of 65 dB or more in the 350-to-1750-nm range. The large dynamic range facilitates source side-mode suppression ratio measurements and light-level measurements on fiber amplifiers.



The analyzer's polarization dependence is only ±0.05 dB or less, and level measurement accuracy is ±0.4 dB or better. Built-in functions include measurement of optical amplifier noise figure. The Advantest Q8383 optical spectrum analyzer also has a power monitor function with a trend-chart dual-screen superimposed display, split-screen display, and three-dimensional display.

The unit's features include a built-in strip chart printer, a plotter interface, an IEEE-488 interface, internal memory, and a 3.5-in. DOS-compatible disk drive. The Q8383 analyzer costs $43,900, with a delivery time of 10 weeks to 12 weeks. JN

Tektronix Inc., P. O. Box 1520, Pittsfield, MA -1202; (800) 426-2200. **CIRCLE 906**

EMULATOR SUPPORTS IBM MC19620 TO 40 MHZ

A real-time emulation system for the MC19620, IBM Microelectronics' high-performance 80196-family derivative, supports the new chip to its top speed of 40 MHz with zero wait states. The device comes in a 100-pin SQFP package that typically is soldered directly to the board, so the emulator, the Model 8800 emulator/analyzer, uses the proprietary Clip-On Emulation scheme with a third-party SQFP test clip and special probing. The system allows users to set, reset, and refine triggers and view successive real-time traces on the fly without breakpoints or wait states. Also available are multilevel triggering, trace filtering, and trace management features. Standard trace size is 16 kframes; 64 kframes is optional. High-level language support is standard. The Model 8800 is hosted by a PC connected by a proprietary parallel interface that allows very fast downloads. The Model 8800 costs $11,850. JN

Orion Instruments Inc., 180 Independence Dr., Menlo Park, CA 94025; (800) 729-7700 or (415) 327-8800. **CIRCLE 907**

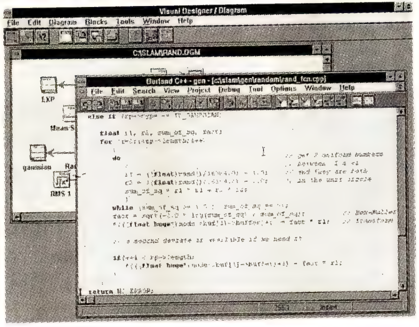
I/O CARD MAXIMIZES DSP BOARD'S THROUGHPUT

A mezzanine I/O card for the UltraDSP VME board supplies the board with a fast enough data stream to take full advantage of the board's Sharp LH9124 DSP engine. The Type-3 module also simplifies cascading of multiple UltraDSP boards for pipelined architectures. With the Type-3 module, the UltraDSP sustains continuous FFT processing rates up to nearly 20 MHz, for block sizes up to 32 kbits. The card uses large 128-kbit-by-48 SRAM buffers to collect an entire data block at once. The result is a dramatic reduction in I/O overhead. Additionally, the card uses hardware techniques to reduce overhead and speed performance. For pipelined processing, the Type-3 module eliminates the need for a time-division-multiplexed data flow. The Type-3 module costs $10,000. JN

Valley Technologies, RD No. 4, Route 309, Tamaqua, PA 18252; (717) 668-3737. **CIRCLE 908**

CREATE CUSTOM WINDOWS APPS FOR DATA ACQUISITION

Because the extensible underlying code enables users to add functions, Visual Designer's custom block toolkit can be expanded to support custom hardware, user-defined algorithms, and special displays. Visual Designer is an application generator for Windows PC-based data acquisition, test, measurement, and control. It uses a graphical user interface so that users can quickly create custom application software for Windows without programming.


Visual Designer / Diagram
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Borland C++ - gen - [c:\slam\gen\random\rand_fcn.cpp]
File Edit Search View Project Debug Tool Options Window Help
EXP
Mean-S
gaussian
RMS 1

The program's wide range of functions include the ability to analyze, display, and output data; stream data to disk and play back data at high speed; control processes and devices; and create custom instruments with chart recorders, panel meter, oscilloscopes, and spectrum analyzers. Parameters such as sample rates, signal ranges, triggering modes, and display or storage options can be specified to meet the exact needs of an application.

The Custom Block Toolkit includes complete examples for math, display, and hardware interfacing. The examples are provided in Microsoft Visual C++, Borland C++, and Symantec C++. Besides these languages, block functions may be written in any language that can generate a Windows DLL (dynamic linked library).

Technical support is available to engineers through the company's BBS or by fax; a year's worth of support is included in the purchase price of $795.

Intelligent Instrumentation, *6550 S. Bay Colony Dr., MS 130, Tucson, AZ 85706; (800) 685-9911; fax (602) 573-0522; BBS (602) 294-7045.* **CIRCLE 909**

■ *SHERRIE VAN TYLE*

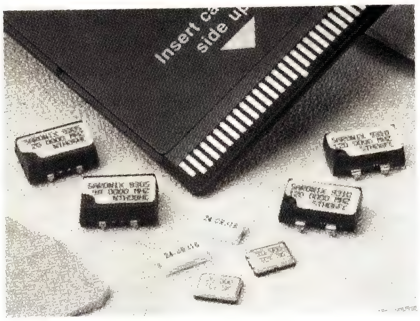
NEURAL NET TOOL DOES EMBEDDED/ONLINE APPS

A Windows-based neural network package has built-in dynamic data exchange (DDE) for Windows applications Excel and Visual Basic. NeuRun for Applications simplifies and speeds developing neural networks that can be queried online for an expert decision or a reaction to input data. It also makes it easier to use Windows' DDE feature. Example programs give the user ready-to-apply templates that can be modified to link a Visual Basic or Excel application with a custom neural network. With Visual Basic, users can generate user-specific functions, such as man-machine interfaces, data loggers, and controllers. Linked by DDE to an online neural network engine, such applications can be made intelligent. As a result, the applications can be used in instrumentation that can react intelligently to changes in data—by raising alarms and shutting down processes. NeuRun for Applications is 99£ (about $150 US in June). A development environment to create an embedded application starts at 385£ (about $583 US in June). SVT

Neural Computer Sciences, Unit 3 Lulworth Business Centre, Nutwood Way, Totton, Southampton SO4 3WW UK; 44 (0) 703 667775; fax -663730. **CIRCLE 910**

DESIGN AND RENDERING SOFTWARE IS UPGRADED

Version 6 of Conceptual Design & Rendering Software has an improved user interface and new rendering features. CDRS version 6 gives several levels of control: During concept development, dynamic sculpting enables designers to work free-form by pushing, pulling, and twisting a surface to define a shape. The model can be refined with boundary influence and surface tangent controls that allow for precise editing of surfaces and tangents as they relate to one another. Surface master/slave relationships control the surface relationships by determining the influence that one shape or surface can exert on another joining surface. Bump-mapping, a new feature, gives enhanced realism of rendered surfaces where textures is part of the object. Designers can toggle between vectors and shaded polygons to verify surfaces fast. Contact the company for prices. SVT



Evans & Sutherland, Design Software Group, 580 Arapeen Dr., Salt Lake City, UT 84108; (801) 582-5847; fax -9413. **CIRCLE 911**

TOOLS EASE CD-ROM PUBLISHING TASKS

Retrieving information from the reams of paper populating files cabinets and stores could be easier with version 2.1 of ZyImage and M/ZyImage document-retrieval tools. The upgrade has been enhanced with new CD-ROM publishing tools and high-volume document imaging features. ZyImage reduces the time it takes to store, retrieve, and distribute paper or electronically based information by combining optical character recognition (OCR), full text retrieval, e-mail, fax, and CD-ROM authoring tools into a complete document imaging and retrieval system. ZyImage 2.1 streamlines data conversion for CD-ROM by scanning and saving text and images directing to Meridian Data Systems' NetScribe CD-ROM authoring products. The ZyImage family includes a data-capture system with scanning, OCR, zoning, templates, editing, electronic file format support, and high-volume options. SVT

ZyLAB, 100 Lexington Dr., Buffalo, IL 60089; (708) 459-8000. **CIRCLE 912**

PRE-MEASURED EPOXY MAKES MIXING EASIER

A convenient 4-gram foil pack makes it easy to mix and bond the EPK 608 epoxy. The quick-set material is suited for a wide range of industrial repair and electronics applications requiring a limited amount of epoxy. The two-compartment foil-pack kit is pre-measured so no weighing or rationing is necessary. It's small enough to be carried in any maintenance or repair kit. The epoxy sets to bond strength in five to 10 minutes, speeding production in electronic applications such as potting and wire harnessing. Call for pricing and delivery information. DM

Hysol Engineering Adhesives, Dexter Distributor Programs, The Dexter Corp., Dept. 5586, One Dexter Dr., Seabrook, NH 03874-4018; (603) 474-5541. CIRCLE 913

EMI GASKETS OFFER IMPROVED QUALITIES

The physical properties of Cho-Seal conductive elastomer EMI-shielding gaskets have been improved. Used in cellular phones and other small electronic packages, the gasket material consists of a silver-filled silicone elastomer applied over a non-conductive silicone tube. The Cho-Seal 3000 gaskets provide 60 dB of shielding effectiveness from 200 MHz to 10 GHz and can be stretched 150% without loss of coating abrasion or electrical conductivity. Their hollow core results in light weight, low closure force, and easy friction-fit retention in grooves. Six diameters are available from 0.040 in. (1.02 mm) to 0.125 in. (3.18 mm). Call for pricing and delivery information. DM

Chomerics Inc., 77 Dragon Ct., Woburn, MA 01888; (617) 935-4850. CIRCLE 914

CERAMIC BALL-GRID ARRAYS SUIT PACKAGING OF FAST, HIGH-POWER ICS

Devices with high clock rates and high power dissipation are candidates for housing in PMC's family of ceramic ball-grid-array (BGA) packages. The high-density packages are an alternative to pin-grid arrays and quad flat packs for ASICs, microprocessors, and other high-performance ICs.

BGAs are a type of IC carrier that connect the IC to a pc board electrically and thermally through an array of solder balls. The package is placed in registration on the board and heated until the balls flow to a limited degree, bonding the device to the board's terminal pads. The short connection paths created handle higher frequencies than do through holes or other surface-mount connections as well as improve signal integrity.

To create its BGA packages, PMC adopted its low-fire ceramic-tape MCM technology. The end result is a package whose internal connections offer transmission-line characteristics with buried passive components for excellent electrical performance. Metal layers can be configured with 50-Ω transmission lines with less than 1 dB insertion loss at 25 GHz and delays of 90 to 180 ps/in. For high-power applications, BGAs can incorporate thermal pipes.

When it comes to board assembly, QFP users often report problems and high rework levels at pitches of 0.5 mm. In contrast, users report six-sigma yields with smaller BGAs that use a larger 1-mm pitch. A QFP with 1225 I/Os at 0.5-mm pitch would require almost 25 in.^{2} of board space. The same device in a 1-mm BGA would take up less than 2 in.^{2}.

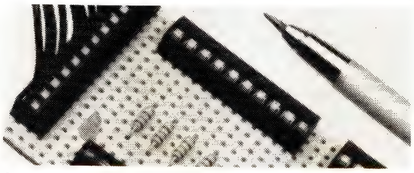
Standard BGAs are available with 40, 156, 304, or 580 balls on an alumina substrate with gold wire-bond pads. Pricing starts at $4.95 in lots of 1000. Samples and production quantities are available now.

Pacific Microelectronics Corp., *10575 S.W. Cascade Blvd., Portland, OR 97223; (800) 622-5574.* CIRCLE 915

■ *DAVID MALINIAK*

PC-BOARD TERMINALS WON'T EAT UP SPACE

In applications where discrete wires must be connected to a pc board but standard-size terminal blocks are too large for available space, the AK550 Series of sub-miniature pc-board terminal blocks may be the answer. The blocks offer a low profile, an extremely small footprint, and density of up to 7 circuits/inch. Pin spacing is 3.5 mm with front or top wire entry. The blocks measure 8.3 mm tall by 6.5 mm deep and are offered with from two to 16 poles. Their tubular screw clamps accept wires from 26 to 16 AWG. Call for pricing, availability, and samples. DM



Altech Corp., 35 Royal Rd., Flemington, NJ 08822-6000; (908) 806-9400. CIRCLE 916

300-LEAD CONNECTOR UNPLUGS IN 2 SECONDS

It takes less than two seconds to mate or unmate the NBY Series cable connectors, which carry from 60 to 300 signal-contact positions. The units employ a 180° cam-action jackscrew and the company's Hypertac low-insertion-force contacts to provide the normal force and cleaning action for reliable operation from dry circuits to 3 A. Termination styles include crimp, pc-board, solder cup, and wire wrap. The 45° plug-cable exit adjusts for varying cable diameters and positive keying provides 36 non-matable variations. Contact resistance is less than 5 mΩ, and the contacts offer virtual immunity to shock and vibration. The connectors are rated for up to 15,000 mating cycles. Prices range from $72 to $193 in lots of 100. Delivery ranges from eight to 10 weeks. DM

Hypertronics Corp., 16 Brent Dr., Hudson, MA 01749; (800) 225-9228. CIRCLE 917

SOFTWARE BRIDGE BLENDS TOOLS FROM MULTIPLE VENDORS INTO ONE WINDOWS-BASED ENVIRONMENT

A multivendor tool suite from the EDA CAD T.E.A.M. uses the company's EDA-Bridge software to tie together tools from Autodesk, Pads Software, and Viewlogic. EDA Office is aimed at designers of pc boards, PLDs, FPGAs, and ASICs. The software runs on PCs under Windows and Windows NT.

The tools in EDA Office are integrated so that they share data throughout the design process using a common database and libraries. Interoperability between tools means that as engineers work, actions performed in one tool are immediately reflected in others. All tools, data, and the process flow are organized and accessible through a common user interface. The user interface makes projects immediately accessible, along with project notes, electronic mail, to-do lists, and office applications.

Because the tools are integrated through a common database, engineers needn't keep track of separate databases, design descriptions, or libraries for each tool. EDA Office tracks which tools are installed, where the appropriate libraries for each tool reside, and how data needs to move between tools as the design passes from one process step to the next. Design databases are automatically read into the common database, where they can be updated from any of the integrated tools. When a design is saved, the data is written in all appropriate native formats.

EDA-Bridge 4.0 with Bridge Speak is integration technology developed by T.E.A.M. Bridge Speak is actually a set of intertool communication messages. It operates as a Windows dynamic link library (DLL), which makes it easy for EDA vendors to add the integration technology to their applications. By embedding Bridge Speak in their EDA applications, any vendor can enable their software to exchange messages and data with other Bridge Speak-compliant applications.

The EDA-Bridge 4.0 software handles all the buffering and communications control. It puts messages and data into a queue, making them available for all participating Bridge Speak applications to receive when ready. EDA-Bridge 4.0 is included in the EDA Office at no additional charge. In other words, applications integrated in EDA Office cost no more than they do when purchased separately.

Another important feature of EDA-Bridge is Corporate Data Link (CDL), a bidirectional, programmable interface to corporate databases. Companies can program CDL to give users access to just those parts of their corporate databases that they need, which is primarily manufacturing-resource-planning systems. Based on the Standard Query Language, CDL gives engineers immediate access to information that's usually difficult to obtain.

EDA Office is available in eight application packages for different types of users. Each package contains EDA-Bridge 4.0 and the specific tools needed by these users—for the same price as the tools alone. Additional tools can be purchased to round out an environment. The eight packages are: PCB Engineer, PLD Engineer, FPGA Engineer, ASIC Engineer, Analog Engineer, Mechanical Engineer, Manufacturing Engineer, and Management Engineer. All products are shipping now. Pricing starts at $995.

***EDA CAD T.E.A.M. Ltd.**, 1731 Technology Dr., Suite 700, San Jose, CA 95110; (408) 437-1313 or (800) 999-1317.* **CIRCLE 918**

■ *LISA MALINIAK*

ESDA SOFTWARE LINKS TO HDL SIMULATORS

The newest release of Vista Technologies' DesignVision electronic-system-design-automation (ESDA) tool can directly interact with third-party hardware-description-language (HDL) simulators. The Verilog version of DesignVision is tightly meshed with Chronologic's Verilog simulator, while the VHDL version links to the Ikos VHDL simulator. DesignVision lets engineers describe their behavioral models with graphics, set simulation breakpoints in the graphical diagrams, display the current simulation state in the diagram, and step through simulation while displaying the changes (animation). Users step forward and backward through simulation time with the system's debugging panel. All conversion between diagram representation and HDL simulation is handled automatically. Also, Vista Technologies will soon offer StateVision, a state-machine editor that directly supports Verilog and VHDL. The tool will read in either of the HDLs to extract information for state-machine models. DesignVision, which runs on Unix workstations, is available now for both Verilog and VHDL. A special deal running through October lets engineers purchase their first copy of the software for only $3000. Regular list price is $10,000. LM

Vista Technologies Inc., 1100 Woodfield Rd., Schaumburg, IL 60173-5124; (708) 706-9300.

CIRCLE 919

HANDLE-BASED EDITOR SIMPLIFIES CAD TOOL

Version 2.0 of the TurboCAD for Windows drawing program features intuitive drag-and-drop handle-based editing. This means that users can now click on a portion of a drawing and stretch, rotate, and move entities with simple mouse movements. Overall, version 2.0 has over 20 new features. These include: global editing of common attributes, bit-mapped fill patterns, vector-based hatching, and an enhanced scripting language. TurboCAD runs on PCs under Microsoft Windows. It's shipping now for $149.95. LM

International Microcomputer Software Inc., 1938 Fourth St., San Rafael, CA 94901; (415) 454-7101. **CIRCLE 920**

NEW LITERATURE

BROCHURE AIDS BUILDERS OF VXIBUS SYSTEMS

A four-page, four-color brochure from the VXIplug&play Alliance contains information on standard frameworks, instrument drivers, soft front panels, and technical support that can help end users develop VXIbus systems.

The brochure discusses system-level issues, such as software, that are not standardized by the baseline VXIbus specification. Then the publication goes on to explain how to build VXIbus systems based on the frameworks endorsed by the VXIplug&play Alliance: DOS, Windows, and graphical Windows.

The free brochure shows how to select a suitable framework and use it to guide the choice of VXIplug-&play-compatible components. The VXIplug&play Alliance, Austin, Texas, was formed to deal with issues beyond the scope of the VXIbus Consortium that affect the integration of multivendor VXIbus systems. JN

CIRCLE 690

CATALOG DESCRIBES IEEE-488 PRODUCTS

A 152-page catalog from IOtech Inc., Cleveland, Ohio, describes hardware and software products for IEEE-488 instrument control and data acquisition. Included are controllers, bus analyzers, bus extenders, serial-to-IEEE-488 converters, and IEEE-488 data-acquisition instruments. New products include hardware and software for IEEE-488 control and notebook PC-based data acquisition. The free catalog describes a driver for Windows NT, a new line of PC-based serial communication boards, and several additions to the DaqBook series of notebook and desktop PC-based portable data-acquisition systems. JN CIRCLE 691

ANALYTICAL INSTRUMENTATION

A 20-page, full-color catalog from George Fischer Signet, Tustin, Calif., features a variety of transmitters, sensors, and controllers designed for ease-of-use in applications ranging from water treatment to chemical processing. Among the products is the new Intelek-Pro Series of Controllers for pH, ORP, and flow, and the company's new Compak housing design made from corrosion-resistant, glass-filled polypropylene.

The company's products include a full range of plastic pipe, fittings, valves, tank linings, heat exchangers, flow and analytical monitoring, and process-control instrumentation. CM CIRCLE 692

SILICON MMICS SELECTION GUIDE

An eight-page Silicon MMICs Product Selection Guide is available from California Eastern Labs, Santa Clara, Calif. It covers NEC's wide range of Silicon IC products, which include wideband amplifiers up to 3.0 GHz, prescalers up to 2.8 GHz, transistor arrays that can be user configured as double-balance mixers or OR/NOR gates, frequency converters, LED drivers, high-isolation amplifiers, and video amplifiers. The guide provides an easy-to use overview of the key electrical characteristics and package dimensions. CM

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SOLUTIONS FOR PORTABLE APPLICATIONS

A 600-page data book from Benchmarq, Carrollton, Texas, describes the company's product focus in four categories. The first category, battery-management ICs, includes battery capacity monitors and single- and dual-battery fast-charge ICs for battery-operated systems. The second category, real-time clock ICs and modules, includes modules that allow users to make inexpensive SRAM nonvolatile for EISA/MCA bus systems, portable PCs, and other applications.

The third category is nonvolatile static and pseudo-static RAM modules, and the fourth category is nonvolatile controller ICs and modules. The free databook includes cross-reference guides and application notes, as well as detailed device specifications, quality methodology, and packaging and ordering information. CM CIRCLE 694

FIBER OPTICS YELLOW PAGES

Information Gatekeepers Inc., Boston, Mass., has released its 1994 edition of the Fiber Optics Yellow Pages directory. The source book contains over 300 pages of useful information on fiber optics, including: a company directory listing over 3000 companies involved in fiber optics, a product index, a geographical index, fiber-optics standard organizations and contact details, sources of information on fiber optics, a 1994 fiber-optics calender of events, and a glossary of terms. Copies of the Fiber Optics Yellow Pages directory are available for $69.95 each. Discounts are available for multiple copies. To order, call the company at (800) 232-1088 or (617) 232-3111. CM CIRCLE 695

SUPERSCOPE II BROCHURE

A 16-page, full-color brochure from GW Instruments, Somerville, Mass., describes SuperScope II, a Macintosh-based software package that can digitize, analyze, calculate, graph, and database waveforms in real time, with the help of data-acquisition hardware available from GW Instruments. SuperScope II includes standard ready-to-go instruments, such as a strip-chart recorder, oscilloscope, spectrum analyzer, and YX recorder. The software can digitize long continuous waveforms, spool them to disk, plot and analyze every point, allow on-line annotation, and then permit post-acquisition viewing. The brochure is available free of charge. CM CIRCLE 696

CONNECTOR SAVVY OUTLINED IN CATALOG

The design and development of interconnects for specific customer applications is the subject of a 16-page, full-color Application Specific Sudden Solution Guide from Samtec Inc., New Albany, Ind. Such interconnects include anything from custom IC-to-board types to simple modifications of standard board-to-board interconnects. Many standard Samtec parts and most of the company's manufacturing capabilities lend themselves to modifications, and this brochure highlights those capabilities. DM CIRCLE 697

SOLVING PROBLEMS IN DEEP SUBMICRON DESIGN

In the May 2 Editorial "Paradigm Shuffle" (p. 16), you question whether current methods are sufficient to deal with simulating deep submicron designs. In particular, you mentioned the issues of nonlinearities and the problems in predicting power dissipation.

We take exception to your remark "Gates are, after all, a figment of our imagination...Gates don't exist in silicon. Transistors do." One could as well remark that transistors don't exist in silicon, electrons and holes do; but then, these are really quantum states, etc.

Physicists develop mathematical models of physical processes and use them, with varied success, to predict the behavior of devices. But they are all just models of underlying physical processes; the real question is what are the appropriate models and calculations that will allow us to predict accurately the behavior of deep submicron devices.

There are roughly three orthogonal problems that are getting significantly more difficult in designing ASICs using deep submicron technology:

1. The complexity of verifying the correct logical operations of a multimillion-transistor design.
2. The modeling complexity of verifying correct timing behavior for designs where parasitic capacitance, inductive coupling, and device linearities are starting to be first-order effects.
3. The difficulty in predicting effective power dissipation in devices where, because of their size and speed, the short-term power dissipation varies wildly over time.

For any single simulation engine to attempt to solve all three of these problems is clearly beyond the computational power of any computer today. The way we are solving these problems is the same way we have always solved difficult engineering problems: We decompose them into orthogonal problems that can be solved independently, and then for each of these we create a hierarchical structure of abstractions that allow us to deal with, ultimately, a small and tractable problem.

In the arena of logic design, we use behavioral and RTL descriptions of systems so that we can deal with system-level and architectural issues, rather than implementation issues. With today's complex, and most demanding systems, architectural design and analysis turns out to be the most important aspect of design. If the system is not correct to start with, then who cares what is finally implemented? It's wrong from the start.

We then use synthesis to generate a gate-level representation of this system, which is verified to be functionally equivalent to the RTL representation. The system's functional correctness is verified at the behavioral and RTL level. To ensure a correct implementation, the gate-level design also must be verified for functional equivalence to the RTL and behavioral levels. Again, sufficient execution of the design must be run to ensure a complete verification. The requirement at the gate level is timing (and thermal) behavior.

Thus, the problems of functional correctness and timing are already being decoupled. In the Zycad engineering group, we use static timing analysis to verify timing, rather than full-timing logic simulation.

This approach is computationally efficient; a particular path's propagation delay needs to be calculated only once to determine whether a design meets its speed goals. This same path must be exercised many times to verify correct logical operation.

The fact that timing analysis is becoming more complex for ASICs is not really a major concern; static timing analysis is a much smaller computational task than logic verification. Even if we need to start modeling timing behavior at the transistor level, and to take into account second-order effects, timing analysis will remain orders of magnitude less demanding computationally than logical verification. Today, we perform signal-integrity verification on our pc boards using a field solver to calculate the electric and magnetic fields on every board trace; this takes only a few hours in a project that lasts months.

Presumably, the problem of power calculations for ASICs could be solved orthogonally from the logical and timing verification of ASICs. Good tools exist today for determining node-toggling behavior from logical simulation without affecting simulation time. This information could be used with static analysis tools to calculate power dissipation over a reasonably wide variety of time scales.

Our personal belief is that the major difficulty in creating ASIC designs that meet their intent will continue to be architectural in nature; that is, specifying the ASIC's behavior as seen by the outside world. We will continue to see the shift of verification cycles into higher levels of abstraction to ensure system correctness as early as possible. Once the chip has been implemented, then the shift will suddenly turn to "does the system work as I defined it?"

We at Zycad understand these problems and are continuing to develop products that address not only today's design requirements but also the next-generation requirements. The Paradigm 2000 Verification Workbench is a set of high-performance tools that allows designers to answer the questions: Is my initial specification correct? Is my implemented design and timing correct? Does the system really work as I planned it?

The cry "the chip works but the system doesn't" will continue to be heard in all too many companies, and the pursuit of system-level specification and verification (functional, timing, and thermal) will be the key to solving these problems. Of all the problems facing system and ASIC designers, these are the ones that are, to the largest degree, "figments of our imagination" but they always have been and will be the most difficult ones we face.

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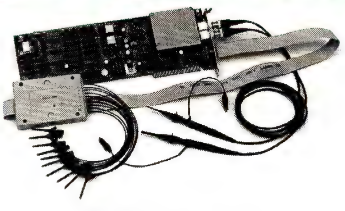

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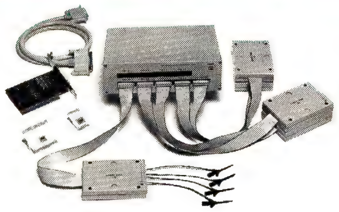

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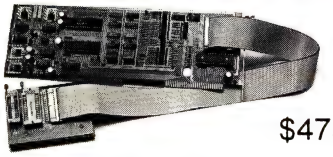

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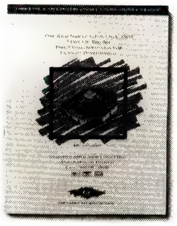

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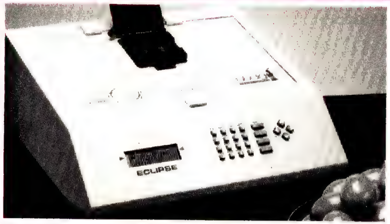

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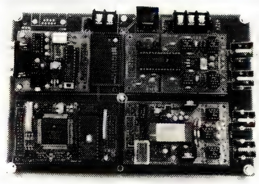

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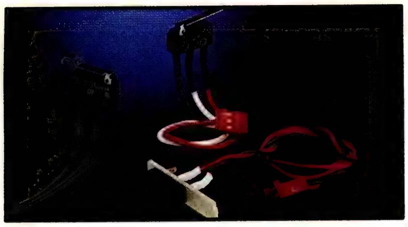

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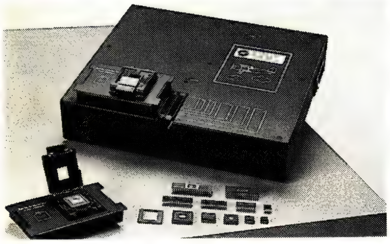

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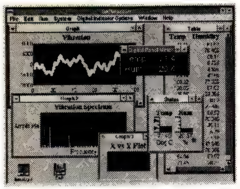

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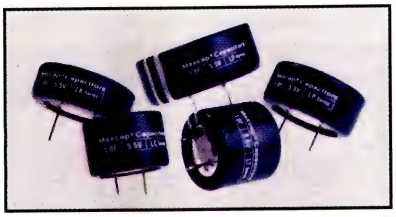

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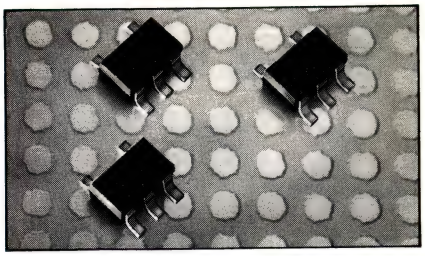

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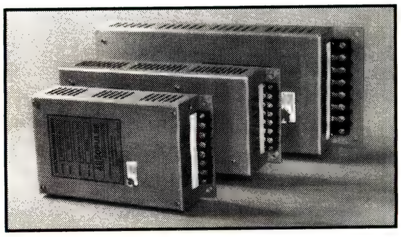

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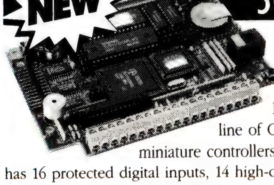

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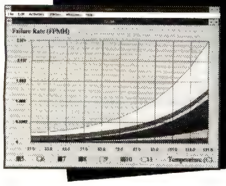

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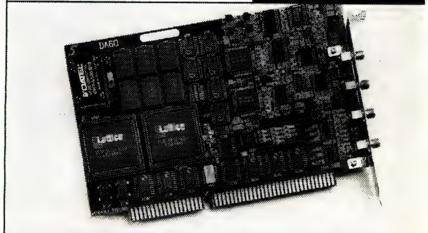

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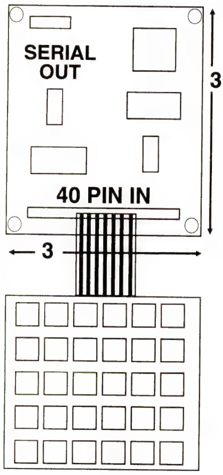

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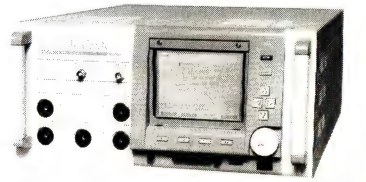

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UPCOMING MEETINGS

JULY

1st IEEE International Workshop on Community Networking, July 13-14. Westin Hotel, San Francisco, CA. Contact Riccardo Guisella, Hewlett-Packard Laboratories., 1501 Page Mill Rd., MS 1 U-17, Palo Alto, CA 94304; (415) 857-7687; fax (415) 857-8526.

1994 IEEE Nuclear & Space Radiation Effects Conference (NSREC), July 18-22. Westin La Paloma Resort, Tucson, AZ. Contact Charles J. Utrias, NSREC vice chairman for publicity, United Technologies, Microelectronics Center, 1575 Garden of the Gods Rd., Colorado Springs, CO 80907; (719) 594-8035; fax (719) 594-8187.

2nd IEEE Workshop on Real-Time Applications, July 21-22. Washington D.C. Contact Alexander D. Stoyenko, Real-Time Computing Lab, Computer & Information Science, New Jersey Institute of Technology, University Heights, Newark, NJ 07102; (201) 596-5765; fax (201) 596-5777; E-mail: Alex@vulcan.njit.edu.

IEEE Power Engineering Society Summer Meeting, July 24-28. Hilton Hotel, San Francisco, CA. Contact Eva Tiffer, Pacific Gas & Electric Co., Mail Code B23C, P.O. Box 770000, San Francisco, CA 94105; (415) 973-2875; fax (415) 972-6011.

AUGUST

3rd IEEE International Symposium on High Performance Distributed Computing, Aug. 3-5. Westin St. Francis Hotel, San Francisco, CA. Contact Geoffrey C. Fox, NPAC Director, Room 3-228, 111 College Pl., Syracuse, NY 13244-4100; (315) 443-4741; fax (315) 443-1973; E-mail: Gcf@pac.syr.edu.

4th IEEE Workshop on Computers in Power Electronics, Aug. 7-10. The Universite du Quebec, Trois-Rivieres, Quebec, Canada. Contact Adam Skorek, Dept. d'Ingenierie, UQTR, C.P. 500, Trois-Rivieres, Quebec G9A 5H7, Canada; (818) 376-5071 ext. 3929; fax (819) 376-5152.

IEEE International Symposium on Applications of Ferroelectrics, Aug. 7-10. Conference Center, University Park, PA. Contact Amar Bhalla, 253 MRL, Pennsylvania State University, University Park, PA 16802; (814) 865-9232.

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '94), Aug. 8-12. California Institute of Technology, Pasadena, CA. Contact Tammy I. Stein, IEEE/GRSS, 2610 Lakeway Dr., Seabrock, TX 77586; (713) 291-9222; fax (713) 291-9224.

IEEE Magnetic Recording Conference (IMRC '94), Aug. 16-20. University of California, La Jolla, CA. Contact Roger F. Hoyt, IBM Almaden Research Center, 650 Harry Rd., K01/803, San Jose, CA 95120-6099; (408) 927-2118; fax (408) 927-3204.

IEEE International Symposium on Electromagnetic Compatibility, Aug. 22-26. Palmer House Hotel, Chicago, IL. Contact H.R. Hofmann, 1210 Lawn Meadow Ln., Naperville, IL 60540; (708) 979-3627; fax (708) 979-5755.

Conference on Lasers & Electro-Optics, Europe & The 5th European Quantum Electronics Convention (CLEO EUROPE/EQEC), Aug. 28-Sept. 2. RAI Congress Centre, Amsterdam, The Netherlands. Contact Susan Evans, IEEE/LEOS, 445 Hoes Ln., P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3896; fax (908) 562-1571.

SEPTEMBER

IEEE International Symposium on Compound Semiconductors, Sept. 18-22. Del Coronado Hotel, San Diego, CA. Contact James Harbison, Bellcore, 331 Newman Springs Rd., Room 3X-211, Red Bank, NJ 07701; (908) 758-3386; fax (908) 758-4372.

14th IEEE International Semiconductor Laser Conference, Sept. 19-23. Hyatt Regency Maui, Maui, HI. Contact Samantha H. Phillips, IEEE/LEOS, 445 Hoes Ln., P.O. Box 1331; (908) 562-3894; fax (908) 562-1571; E-mail: s.phillips@ieee.org.

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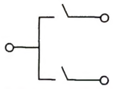

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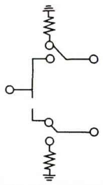

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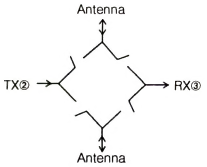

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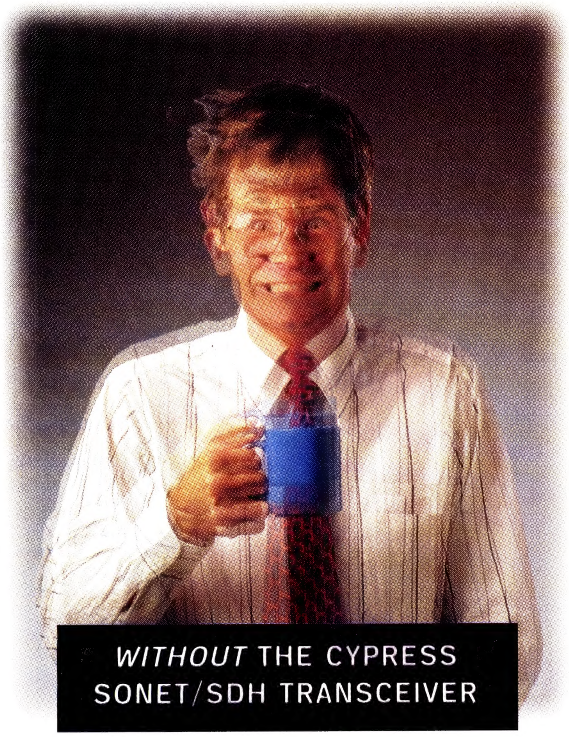
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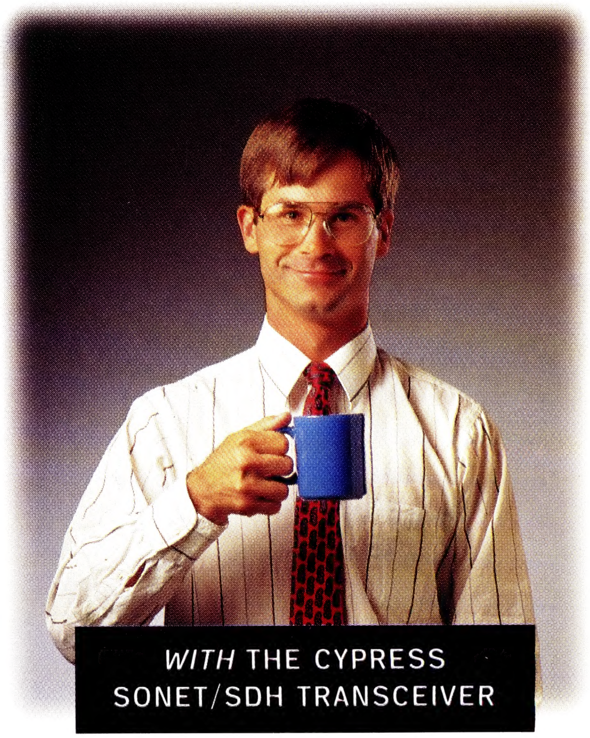
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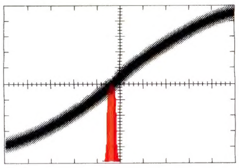
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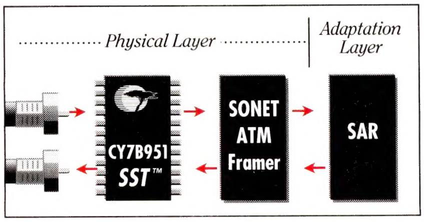

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